1. Record Nr. UNINA9910782299303321

Autore	Goldman Stanley J.
Titolo	Phase-locked loop engineering handbook for integrated circuits / / Stanley Goldman
Pubbl/distr/stampa	Boston : , : Artech House, , ©2007 [Piscataqay, New Jersey] : , : IEEE Xplore, , [2007]
ISBN	1-59693-155-8
Descrizione fisica	1 online resource (572 p.)
Collana	Artech House microwave library
Disciplina	621.3815364
Soggetti	Integrated circuits - Design and construction Phase-locked loops
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Phase-Locked Loop Engineering Handbook for Integrated Circuits; Contents vii; Preface xiii; Acknowledgments xxi; Chapter 1 Getting Started with PLLs 1; Chapter 2 System Analysis 15; Chapter 3 System Requirements 35; Chapter 4 Components, Part 1-Dividers and Oscillators 163; Chapter 5 Components, Part 2-Detectors and Other Circuits 235; Chapter 6 Loop-Compensation Synthesis Revisited 307; Chapter 7 Test and Measurement 353; Chapater 8 Simulation 405; Chapter 9 Applications and Extensions 445; Appendix A Letter Symbols 529; Appendix B Glossary 533; About the Author 541; Index 543
Sommario/riassunto	Phased-locked loops (PLLs) are control systems that have become indispensable in today's electronic circuitry. This highly accessible handbook is an practical resource that electronics engineers and circuit designers will find invaluable when developing these systems. PLLs are highly complex to design and are just as difficult to test. To speed development and ensure effective testing, engineers can turn to this collection of practical solutions, SPICE listings, simulation techniques, and testing set-ups. The book offers in-depth coverage of monolithic phase-locked loops and the latest generat.