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Nota di contenuto	Metamodeling-Driven IP Reuse for SoC Integration and Microprocessor Design; Contents; Preface; References; Acknowledgments; Chapter 1 Introduction; Design IP; Verification IP; Design Reuse; Verification Reuse; 1.1 ONGOING EFFORTS IN DESIGN IP REUSE; 1.2 ONGOING EFFORTS IN VERIFICATION IP REUSE; 1.3 ESSENTIAL ISSUES WITH IP REUSE; Essential Issues with Design IP Reuse; (1) IP Provider; IP Library; Documentation; Quality Assurance; Standardization; (2) IP Integrator; Exploration; Integration; Methodology and Environment; (3) Tool Developer for IP Reuse; Support for IP Provider Support for IP IntegratorEssential Issues with Verification IP Reuse; (1) Modeling Language; (2) Generation Algorithms; 1.4 METAMODELING APPROACH TO REUSE; 1.5 PROBLEM STATEMENT; 1.6 RESEARCH CONTRIBUTIONS; 1.7 TOOLS AND TECHNIQUES DEVELOPED; References; Chapter 2 Background; 2.1 METAMODELING; 2.1.1 Implicit Metamodeling Versus Explicit Metamodeling; 2.1.2 Generic Modeling Environment; 2.2 COMPONENT COMPOSITION FRAMEWORK; 2.3

REFLECTION AND INTROSPECTION (R-I); 2.4 SYSTEMC; 2.5 MODEL-DRIVEN VALIDATION; 2.5.1 Microprocessor Validation Flow; 2.5.2 Simulation-Based Functional Validation
2.6 TEST GENERATION2.6.1 Constraint Programming; 2.6.2 Esterel Studio; 2.7 COVERAGE-DIRECTED TEST GENERATION; 2.7.1 Structural Coverage; 2.7.2 Functional Coverage; 2.7.3 Property Specification Language (PSL); 2.7.4 Fault Classification; References; Chapter 3 Related Work; 3.1 COMPONENT COMPOSITION FRAMEWORK; 3.1.1 The BALBOA Framework; 3.1.2 Liberty Simulation Environment (LSE); 3.1.3 EWD; 3.1.4 Ptolemy II; 3.1.5 Metropolis; 3.2 COMPONENT-BASED SOFTWARE DESIGN ENVIRONMENTS; 3.3 IP INTERFACING STANDARDS; 3.3.1 SPIRIT; 3.4 EXISTING TOOLS FOR STRUCTURAL REFLECTION
3.5 ARCHITECTURE DESCRIPTION LANGUAGES3.6 TEST GENERATION; References; Part I Design Reuse; Chapter 4 A Metamodel for Component Composition; 4.1 CC LANGUAGE, METAMODEL, AND MODEL; 4.1.1 Component Composition Language (CCL); 4.1.2 Component Composition Metamodel (CCMM); 4.1.3 Component Composition Model (CCM); 4.2 CC ANALYSIS AND TRANSLATION; 4.2.1 Consistency Checking; 4.2.2 Type Inference; 4.2.3 XML Translation; 4.3 CASE STUDIES; 4.3.1 AMBA AHB RTL Bus Model; 4.3.2 Simple Bus TL Model; 4.4 DESIGN EXPERIENCE AND SUMMARY; References; Chapter 5 IP Reflection and Selection
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Sommario/riassunto

This cutting-edge resource offers you an in-depth understanding of metamodeling approaches for the reuse of intellectual properties (IPs) in the form of reusable design or verification components. The book covers the essential issues associated with fast and effective integration of reusable design components into a system-on-a-chip (SoC) to achieve faster design turn-around time. Moreover, it addresses key factors related to the use of reusable verification IPs for a "write once, use many times" verification strategy - another effective approach that can attain a faster product design cycle.