1.

Record Nr.	UNINA9910780935303321
Autore	Mathaikutty Deepak A.
Titolo	Metamodeling-driven IP reuse for SoC integration and microprocessor design / / Deepak A. Mathaikutty, Sandeep K. Shukla
Pubbl/distr/stampa	Boston : , : Artech House, , ©2009 [Piscataqay, New Jersey] : , : IEEE Xplore, , [2009]
ISBN	1-59693-425-5
Descrizione fisica	1 online resource (310 p.)
Altri autori (Persone)	ShuklaSandeep K
Disciplina	621.39 621.3916
Soggetti	Computer software - Reusability Computer software - Verification Intellectual property Microprocessors - Design and construction System design Systems on a chip - Design and construction
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Metamodeling-Driven IP Reuse for SoC Integration and Microprocessor Design; Contents; Preface; References; Acknowledgments; Chapter 1 Introduction; Design IP; Verification IP; Design Reuse; Verification Reuse; 1.1 ONGOING EFFORTS IN DESIGN IP REUSE; 1.2 ONGOING EFFORTS IN VERIFICATION IP REUSE; 1.3 ESSENTIAL ISSUES WITH IP REUSE; Essential Issues with Design IP Reuse; (1) IP Provider; IP Library; Documentation; Quality Assurance; Standardization; (2) IP Integrator; Exploration; Integration; Methodology and Environment; (3) Tool Developer for IP Reuse; Support for IP Provider Support for IP IntegratorEssential Issues with Verification IP Reuse; (1) Modeling Language; (2) Generation Algorithms; 1.4 METAMODELING APPROACH TO REUSE; 1.5 PROBLEM STATEMENT; 1.6 RESEARCH CONTRIBUTIONS; 1.7 TOOLS AND TECHNIQUES DEVELOPED; References; Chapter 2 Background; 2.1 METAMODELING; 2.1.1 Implicit Metamodeling Versus Explicit Metamodeling; 2.1.2 Generic Modeling Environment; 2.2 COMPONENT COMPOSITION FRAMEWORK; 2.3

Sommario/riassunto

This cutting-edge resource offers you an in-depth understanding of metamodeling approaches for the reuse of intellectual properties (IPs) in the form of reusable design or verification components. The book covers the essential issues associated with fast and effective integration of reusable design components into a system-on-a-chip (SoC) to achieve faster design turn-around time. Moreover, it addresses key factors related to the use of reusable verification IPs for a "write once, use many times" verification strategy - another effective approach that can attain a faster product design cycle.