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	Model; 4.2.3 Serial I/O Example 2: Networking and Communications: IEEE 802.11 Wireless LAN; 4.2.4 Parallel I/O; 4.2.5 Parallel I/O Example 3: ""Parallel"" Output and Graphics I/O 4.2.6 Parallel and Serial I/O Example 4: Networking and Communications-Ethernet4.2.7 Example 1: Motorola/Freescale MPC823 FADS Board Ethernet System Model; 4.2.8 Example 2: Net Silicon ARM7 (6127001) Development Board Ethernet System Model; 4.2.9 Example 3: Adastra Neptune x86 Board Ethernet System Model; 4.3 Interfacing the I/O Components; 4.3.1 Interfacing the I/O Device with the Embedded Board; 4.3.2 Interfacing an I/O Controller and the Master CPU; 4.4 I/O and Performance; 4.5 Board Buses; 4.6 Bus Arbitration and Timing; 4.6.1 Nonexpandable Bus: I[sup(2)]C Bus Example
	 4.6.2 PCI (Peripheral Component Interconnect) Bus Example: Expandable4.7 Integrating the Bus with Other Board Components; 4.8 Bus Performance; Chapter 5 Memory Systems; 5.1 Introduction; 5.2 Memory Spaces; 5.2.1 L1 Instruction Memory; 5.2.2 Using L1 Instruction Memory for Data Placement; 5.2.3 L1 Data Memory; 5.3 Cache Overview; 5.3.1 What Is Cache?; 5.3.2 Direct-Mapped Cache; 5.3.3 Fully Associative Cache; 5.3.4 N-Way Set-Associative Cache; 5.3.5 More Cache Details; 5.3.6 Write-Through and Write-Back Data Cache; 5.4 External Memory; 5.4.1 Synchronous Memory; 5.4.2 Asynchronous Memory 5.4.3 Nonvolatile Memories
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