1. Record Nr. UNINA9910768476203321

Titolo	Formal Methods for Hardware Verification : 6th International School on Formal Methods for the Design of Computer, Communication, and Software Systems, SFM 2006, Bertinoro, Italy, May 22-27, 2006, Advances Lectures / / edited by Marco Bernardo, Alessandro Cimatti
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2006
ISBN	3-540-34305-9
Edizione	[1st ed. 2006.]
Descrizione fisica	1 online resource (VIII, 244 p.)
Collana	Programming and Software Engineering, , 2945-9168 ; ; 3965
Altri autori (Persone)	CimattiAlessandro BernardoMarco
Disciplina	004.01/51
Soggetti	Computer science Software engineering Compilers (Computer programs) Computers, Special purpose Computer networks Theory of Computation Software Engineering Compilers and Interpreters Computer Science Logic and Foundations of Programming Special Purpose and Application-Based Systems Computer Communication Networks
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Hardware Design and Simulation for Verification -- Automatic Test Pattern Generation -- An Introduction to Symbolic Trajectory Evaluation -- BDD-Based Hardware Verification -- SAT-Based Verification Methods and Applications in Hardware Verification -- Building Efficient Decision Procedures on Top of SAT Solvers -- Refinement and Theorem Proving -- Floating-Point Verification Using Theorem Proving.
Sommario/riassunto	This book presents 8 papers accompanying the lectures of leading researchers given at the 6th edition of the International School on

Formal Methods for the Design of Computer, Communication and Software Systems (SFM 2006). SFM 2006 was devoted to formal techniques for hardware verification and covers several aspects of the hardware design process, including hardware design languages and simulation, property specification formalisms, automatic test pattern generation, symbolic trajectory evaluation, and more.