

1. Record Nr.	UNINA9910768457503321
Titolo	Field-Programmable Logic and Applications : 11th International Conference, FPL 2001, Belfast, Northern Ireland, UK, August 27-29, 2001 Proceedings // edited by Gordon Brebner, Roger Woods
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2001
ISBN	3-540-44687-7
Edizione	[1st ed. 2001.]
Descrizione fisica	1 online resource (XV, 665 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 2147
Disciplina	621.39/5
Soggetti	Computer architecture Software engineering Computer networks Logic design Microprocessors Computer-aided engineering Computer System Implementation Software Engineering/Programming and Operating Systems Computer Communication Networks Logic Design Processor Architectures Computer-Aided Engineering (CAD, CAE) and Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
Nota di contenuto	Invited Keynote 1 -- Technology Trends and Adaptive Computing -- Architectural Frameworks -- Prototyping Framework for Reconfigurable Processors -- An Emulator for Exploring RaPiD Configurable Computing Architectures -- Place and Route 1 -- A New Placement Method for Direct Mapping into LUT-Based FPGAs -- fGREP - Fast Generic Routing Demand Estimation for Placed FPGA Circuits -- Architecture -- Macrocell Architectures for Product Term Embedded Memory Arrays -- Gigahertz Reconfigurable Computing Using SiGe HBT BiCMOS FPGAs -- Memory Synthesis for FPGA-Based Reconfigurable Computers -- DSP 1

-- Implementing a Hidden Markov Model Speech Recognition System in Programmable Logic -- Implementation of (Normalised) RLS Lattice on Virtex -- Accelerating Matrix Product on Reconfigurable Hardware for Signal Processing -- Synthesis -- Static Profile-Driven Compilation for FPGAs -- Synthesizing RTL Hardware from Java Byte Codes -- PuMA++: From Behavioral Specification to Multi-FPGA-Prototype -- Encryption -- Secure Configuration of Field Programmable Gate Arrays -- Single-Chip FPGA Implementation of the Advanced Encryption Standard Algorithm -- JBits™ Implementations of the Advanced Encryption Standard (Rijndael) -- Runtime Recon.guration 1 -- Task-Parallel Programming of Reconfigurable Systems -- Chip-Based Reconfigurable Task Management -- Configuration Caching and Swapping -- Graphics and Vision -- Multiple Stereo Matching Using an Extended Architecture -- Implementation of a NURBS to Bézier Conversor with Constant Latency -- Reconfigurable Frame-Grabber for Real-Time Automated Visual Inspection (RT-AVI) Systems -- Invited Keynote 2 -- Processing Models for the Next Generation Network -- Place and Route 2 -- Tightly Integrated Placement and Routing for FPGAs -- Gambit: A Tool for the Simultaneous Placement and Detailed Routing of Gate-Arrays -- Networking -- Reconfigurable Router Modules Using Network Protocol Wrappers -- Development of a Design Framework for Platform-Independent Networked Reconfiguration of Software and Hardware -- Processor Interaction -- The MOLEN ??-Coded Processor -- Run-Time Optimized Reconfiguration Using Instruction Forecasting -- CRISP: A Template for Reconfigurable Instruction Set Processors -- Applications -- Evaluation of an FPGA Implementation of the Discrete Element Method -- Run-Time Performance Optimization of an FPGA-Based Deduction Engine for SAT Solvers -- A Reconfigurable Embedded Input Device for Kinetically Challenged Persons -- Methodology 1 -- Bubble Partitioning for LUT-Based Sequential Circuits -- Rapid Construction of Partial Configuration Datastreams from High-Level Constructs Using JBits -- Placing, Routing, and Editing Virtual FPGAs -- DSP 2 -- Virtex Implementation of Pipelined Adaptive LMS Predictor in Electronic Support Measures Receiver -- A Music Synthesizer on FPGA -- Motivation from a Full-Rate Specific Design to a DSP Core Approach for GSM Vocoders -- Loops and Systolic -- Loop Tiling for Reconfigurable Accelerators -- The Systolic Ring: A Dynamically Reconfigurable Architecture for Embedded Systems -- A n-Bit Reconfigurable Scalar Quantiser -- Image Processing -- Real Time Morphological Image Contrast Enhancement in Virtex FPGA -- Demonstrating Real-time JPEG Image Compression-Decompression using Standard Component IP Cores on a Programmable Logic based Platform for DSP and Image Processing -- Design and Implementation of an Accelerated Gabor Filter Bank Using Parallel Hardware -- Invited Keynote 3 -- The Evolution of Programmable Logic: Past, Present, and Future Predictions -- Runtime Reconfiguration 2 -- Dynamically Reconfigurable Cores -- Reconfigurable Breakpoints for Co-debug -- Faults -- Using Design-Level Scan to Improve FPGA Design Observability and Controllability for Functional Verification -- FPGA-Based Fault Injection Techniques for Fast Evaluation of Fault Tolerance in VLSI Circuits -- Methodology 2 -- A Generic Library for Adaptive Computing Environments -- Generative Development System for FPGA essors with Active Components -- Compilation Increasing the Scheduling Scope for Multi-memory-FPGA-Based Custom Computing Machines -- System Level Tools for DSP in FPGAs -- Arithmetic -- Parameterized Function Evaluation for FPGAs -- Efficient Constant Coefficient Multiplication Using Advanced FPGA Architectures -- A Digit-Serial Structure for Reconfigurable Multipliers -- FPGA Resource Reduction Through Truncated Multiplication -- Short

Papers 1 -- Efficient Mapping of Pre-synthesized IP-Cores onto Dynamically Reconfigurable Array Architectures -- An FPGA-Based Syntactic Parser for Real-Life Almost Unrestricted Context-Free Grammars -- Hardware-Software Partitioning: A Reconfigurable and Evolutionary Computing Approach -- An Approach to Real-Time Visualization of PIV Method with FPGA -- FPGA-Based Discrete Wavelet Transforms System -- X-MatchPRO: A ProASIC-Based 200 Mbytes/s Full-Duplex Lossless Data Compressor -- Arithmetic Operation Oriented Reconfigurable Chip: RHW -- Short Papers 2 -- Initial Analysis of the Proteus Architecture -- Building Asynchronous Circuits with JBits -- Case Study of Integration of Reconfigurable Logic as a Coprocessor into a SCI-Cluster under RT-Linux -- A Reconfigurable Approach to Packet Filtering -- FPGA-Based Modelling Unit for High Speed Lossless Arithmetic Coding -- A Data Re-use Based Compiler Optimization for FPGAs -- Dijkstra's Shortest Path Routing Algorithm in Reconfigurable Hardware -- A System on Chip for Power Line Communications According to European Home Systems Specifications.

Sommario/riassunto

This book constitutes the refereed proceedings of the 11th International Conference on Field-Programmable Logic and Application, FPL 2001, held in Belfast, Northern Ireland, UK, in August 2001. The 56 revised full papers and 15 short papers presented were carefully reviewed and selected from a total of 117 submissions. The book offers topical sections on architectural framework, place and route, architecture, DSP, synthesis, encryption, runtime reconfiguration, graphics and vision, networking, processor interaction, applications, methodology, loops and systolic, image processing, faults, and arithmetic.
