1. Record Nr. UNINA9910767569803321

Titolo	Algorithm Engineering and Experimentation : International Workshop ALENEX'99 Baltimore, MD, USA, January 15-16, 1999, Selected Papers / / edited by Michael T. Goodrich, Catherine C. McGeoch
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 1999
ISBN	3-540-48518-X
Edizione	[1st ed. 1999.]
Descrizione fisica	1 online resource (VIII, 356 p.)
Collana	Lecture Notes in Computer Science, , 1611-3349 ; ; 1619
Disciplina	005.1
Soggetti	Computer programming Data structures (Computer science) Information theory Application software Algorithms Artificial intelligence - Data processing Computer graphics Programming Techniques Data Structures and Information Theory Computer and Information Systems Applications Data Science Computer Graphics
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Combinatorial Algorithms -- Efficient Implementation of the WARM-UP Algorithm for the Construction of Length-Restricted Prefix Codes -- Implementing Weighted b-Matching Algorithms: Insights from a Computational Study -- Designing Practical Efficient Algorithms for Symmetric Multiprocessors -- Circular Drawings of Biconnected Graphs -- Heuristics and Experimental Design for Bigraph Crossing Number Minimization -- Binary Space Paritions in Plücker Space -- Practical Point-in-Polygon Tests Using CSG Representations of Polygons -- Software and Applications -- Accessing the Internal Organization of

Data Structures in the JDSL Library -- Object-Oriented Design of Graph Oriented Data Structures -- A Case Study on the Cost of Geometric Computing -- Design and Implementation of the Fiduccia-Mattheyses Heuristic for VLSI Netlist Partitioning -- Algorithms for Restoration Planning in a Telecommunications Network -- Computing the n × m Shortest Paths Efficiently -- Image Watermarking for Copyright Protection -- Algorithms for NP-Hard Problems -- A Self Organizing Bin Packing Heuristic -- Finding the Right Cutting Planes for the TSP -- Obstacle-Avoiding Euclidean Steiner Trees in the Plane: An Exact Algorithm -- Data Structures -- Adaptive Algorithms for Cache-efficient Trie Search -- Fast Priority Queues for Cached Memory -- Efficient Bulk Operations on Dynamic R-trees.

Sommario/riassunto

Symmetric multiprocessors (SMPs) dominate the high-end server market and are currently the primary candidate for constructing large scale multiprocessor systems. Yet, the design of e cient parallel algorithms for this platform c- rently poses several challenges. The reason for this is that the rapid progress in microprocessor speed has left main memory access as the primary limitation to SMP performance. Since memory is the bottleneck, simply increasing the n- ber of processors will not necessarily yield better performance. Indeed, memory bus limitations typically limit the size of SMPs to 16 processors. This has at least twoimplicationsfor the algorithmdesigner. First, since there are relatively few processors availableon an SMP, any parallel algorithm must be competitive with its sequential counterpart with as little as one processor in order to be r- evant. Second, for the parallel algorithm to scale with the number of processors, it must be designed with careful attention to minimizing the number and type of main memory accesses. In this paper, we present a computational model for designing e cient al- rithms for symmetric multiprocessors. We then use this model to create e cient solutions to two widely di erent types of problems - linked list pre x com- tations and generalized sorting. Both problems are memory intensive, but in die rent ways. Whereas generalized sorting algorithms typically require a large numberofmemoryaccesses, they areusuallytocontiguousmemorylocations. By contrast, prex computation algorithms typically require a more modest qu- tity of memory accesses, but they are are usually to non-contiguous memory locations.