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Nota di contenuto	Chapter 1. Introduction -- Chapter 2. Preliminaries -- Chapter 3. Exploring Circuit Design Topologies for RFETs -- Chapter 4. Standard Cells and Technology Mapping -- Chapter 5. Logic Synthesis with XOR-Majority Graphs -- Chapter 6. Physical synthesis flow and liberty generation -- Chapter 7. Polymporphic Primitives for Hardware Security -- Chapter 8. Conclusion.
Sommario/riassunto	This book is a single-source solution for anyone who is interested in exploring emerging reconfigurable nanotechnology at the circuit level. It lays down a solid foundation for circuits based on this technology having considered both manual as well as automated design flows. The authors discuss the entire design flow, consisting of both logic and physical synthesis for reconfigurable nanotechnology-based circuits. The authors describe how transistor reconfigurable properties can be exploited at the logic level to have a more efficient circuit design flow, as compared to conventional design flows suited for CMOS. Further, the book provides insights into hardware security features that can be

intrinsically developed using the runtime reconfigurable features of this nanotechnology. Details an entire design automation flow for building circuits based on emerging reconfigurable nanotechnology; Describes logical abstraction for emerging reconfigurable nanotechnology that is essential for building newer circuits; Presents hardware security solutions that use reconfigurable nanotechnology to complement contemporary CMOS circuits.