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| Nota di contenuto | Intro -- Preface -- Acknowledgments -- Contents -- About the |

Authors -- Abbreviations -- Chapter 1: Introduction -- 1.1 DDS Technology Overview -- 1.2 Application Fields of DDS -- 1.3 A 2.5 GHz DDS Design Case Introduced in This Book -- Block Functions Introduction -- Design Process Introduction -- References -- Chapter 2: Phase to Amplitude Converter -- 2.1 Introduction -- 2.2 Implementation Technology of Phase to Amplitude Conversion -- ROM Look-Up Table Technology -- Nonlinear DAC Technology -- Analog Mode Conversion Technology -- Angle Decomposition Technology -- ROM Compression Technology -- Polynomial Approximation Technology -- Coordinated Rotation Digital Computer (CORDIC) Algorithm Technology -- 2.3 Considerations of CORDIC Algorithm in Circuit Implementation -- Phase Truncation -- Symmetry and Segmentation of Sine Wave -- Eliminate Rotation Sign Judgement -- Offset Pre-rotation Operation -- Decrease the Number of Rotation -- 2.4 Design Case of An Optimized Excess-Four CORDIC Algorithm -- Optimization Scheme of Excess-Four Algorithm -- High Speed Parallel Architecture Based on Linear Phase Interpolation -- Measurement Results and Comparison -- 2.5 Summary -- References -- Chapter 3: High Speed Current Steering D/A Converter -- 3.1 Introduction -- 3.2 Several Design Technologies -- Design Technologies to Deal with Current Source Mismatch -- Design Technologies to Deal with Finite Output Impedance -- Design Technologies to Deal with Non-ideal MOS Switch State -- Design Technologies to Deal with Charge Feed Through of the Switch -- Design Technologies to Deal with Code Dependent Clock Load -- Design Technologies to Deal with Code Dependent Nonlinear Glitch -- Design Technologies to Deal with Code Dependent Nonlinear Memory -- Summary -- 3.3 Problems Related to High Speed DAC Design -- 3.4 Design Case of a Built-In 14 Bit DAC in 2.5 GHz DDS. Introduction -- Bias Circuit of PMOS Cascode Current Source Array -- Re-sampler and Driver Circuit -- 8 to 1 MUX Circuit -- DEM -- Layout Scheme -- Simulation Verification Scheme -- Measurement Results and Comparison -- 3.5 Summary -- References -- Chapter 4: Other Functional Modules -- 4.1 Phase Accumulator -- 4.2 Digital Spurious Cancellation Module -- Introduction -- Amplitude and Phase Quantization Effect -- Implementation scheme of Digital Spurious Cancellation in DDS Chip -- Digital Spurious Cancellation Procedure and Measurement Results -- 4.3 Multi-chip Synchronization Module -- The Origin of Multi-chip Synchronization Problem -- Conventional Multi-chip Synchronization Circuit -- Several Published Multi-chip Synchronization Circuit Scheme -- A Multi-chip Synchronization Circuit Scheme Based on Diversity Technique -- 4.4 Profile Register Module -- 4.5 Linear Sweep Module -- 4.6 Summary -- References -- Chapter 5: Summary and Outlook.
