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	Nota di contenuto	2nd International Workshop on Malleability Techniques Applications in High-Performance Computing (HPCMALL) -- From Static to Malleable: Improving Flexibility and Compatibility in Burst Buffer File Systems -- Malleable techniques and resource scheduling to improve energy efficiency in parallel applications -- Towards Achieving Transparent Malleability Thanks to MPI Process Virtualization -- A Case Study on PMIx-usage for Dynamic Resource Management -- Malleable and adaptive ad-hoc file system for data intensive workloads in HPC applications -- Malleable and adaptive ad-hoc file system for data intensive workloads in HPC applications -- Towards Smarter Schedulers: Molding Jobs into the Right Shape via Monitoring and Modeling -- 18th Workshop on Virtualization in High-Performance Cloud Computing (VHPC 23) -- Improving live migration efficiency in QEMU: a paravirtualized approach -- Performance losses with virtualization: Comparing bare metal to VMs and containers -- Real-

Time Unikernels: a First Look -- Accelerating Scientific Applications with the Quantum Edge: a Drug Design Use Case -- Event-Driven Chaos Testing For Containerized Applications -- HPC I/O in the Data Center (HPC IODC) -- Analyzing Parallel Applications for Unnecessary I/O Semantics That Inhibit File System Performance -- Workshop on Converged Computing of Cloud, HPC, and Edge (WOCC'23) -- Running Kubernetes Workloads on HPC -- A GPU-accelerated Molecular Docking Workflow with Kubernetes and Apache Airflow -- Cloud-Bursting and Autoscaling for Python-Native Scientific Workflows Using Ray -- Understanding System Resilience for Converged Computing of Cloud, Edge, and HPC -- Estimating the Energy Consumption of Applications in the Computing Continuum with iFogSim -- 7th International Workshop on In Situ Visualization (WOIV'23) -- Inshimtu – A Lightweight In Situ Visualization "Shim" -- Catalyst-ADIOS2: in transit analysis for numerical simulations using Catalyst 2 API -- A Case Study on Providing Accessibility-Focused In-Transit Architectures for Neural Network Simulation and Analysis -- Workshop on Monitoring and Operational Data Analytics (MODA23) -- Automatic Detection of HPC Job Inefficiencies at TU Dresden's HPC center with PIKA -- ML-based methodology for HPC facilities supervision -- A Fast Simulator to Enable HPC Scheduling Strategy Comparisons -- 2nd Workshop on Communication, I/O, and Storage at Scale on Next-Generation Platforms: Scalable Infrastructures -- Application Performance Analysis: a Report on the Impact of Memory Bandwidth -- DAOS beyond Persistent Memory: Architecture and Initial Performance Results -- Enabling Multi-level Network Modeling in Structural Simulation Toolkit for Next-Generation HPC Network Design Space Exploration -- Portability and Scalability of OpenMP Offloading on State-of-the-art Accelerators -- An Earlier Experiences towards Optimizing Apache Spark over Frontera Supercomputer -- Bandwidth Limits in the Intel Xeon Max (Sapphire Rapids with HBM) Processors -- First International Workshop on RISC-V for HPC -- Test-driving RISC-V Vector hardware for HPC -- Backporting RISC-V Vector assembly -- Functional Testing with STLs: A Step Towards Reliable RISC-V-based HPC Commodity Clusters -- Challenges and Opportunities for RISC-V Arquitectures towards Genomics-based Workloads -- Optimizations for Very Long and Sparse Vector Operations on a RISC-V VPU : A Work-in-progress -- Performance Modelling-driven Optimization of RISC-V Hardware for Efficient SpMV -- Prototyping reconfigurable RRAM-based AI accelerators using the RISC-V ecosystem and Digital Twins -- Optimization of the FFT algorithm on RISC-V CPUs -- Software Development Vehicles to enable extended and early co-design: a RISC-V and HPC case of study -- Evaluation of HPC Workloads Running on Open-Source RISC-V Hardware -- Accelerating Neural Networks using Open Standard Software on RISC-V -- Second Combined Workshop on Interactive and Urgent Supercomputing (CWIUS) -- From Desktop to Supercomputer: Computational Fluid Dynamics Augmented by Molecular Dynamics using MaMiCo and preCICE -- Open OnDemand Connector for Amazon Elastic Kubernetes Service -- HPC on Heterogeneous Hardware (H3) -- GEMM-Like Convolution for Deep Learning Inference on the Xilinx Versal -- An Investigation into the Performance and Portability of SYCL Compiler Implementations -- Observed Memory Bandwidth and Power Usage on FPGA Platforms with oneAPI and Vitis HLS: A Comparison with GPUs -- Evaluating Quantum Algorithms for Linear Algebra Workflows -- Exploring the Use of Dataflow Architectures for Graph Neural Network Workloads -- OpenACC unified programming environment for multi-hybrid acceleration HPC with GPU and FPGA.

Sommario/riassunto

This volume constitutes the papers of several workshops which were held in conjunction with the 38th International Conference on High Performance Computing, ISC High Performance 2023, held in Hamburg, Germany, during May 21–25, 2023. The 49 revised full papers presented in this book were carefully reviewed and selected from 70 submissions. ISC High Performance 2023 presents the following workshops: 2nd International Workshop on Malleability Techniques Applications in High-Performance Computing (HPCMALL) 18th Workshop on Virtualization in High-Performance Cloud Computing (VHPC 23) HPC I/O in the Data Center (HPC IODC) Workshop on Converged Computing of Cloud, HPC, and Edge (WOCC'23) 7th International Workshop on In Situ Visualization (WOIV'23) Workshop on Monitoring and Operational Data Analytics (MODA23) 2nd Workshop on Communication, I/O, and Storage at Scale on Next-Generation Platforms: Scalable Infrastructures First International Workshop on RISC-V for HPC Second Combined Workshop on Interactive and Urgent Supercomputing (CWIUS) HPC on Heterogeneous Hardware (H3).