

|                         |   |
|-------------------------|---|
| 1. Record Nr.           | UNINA9910739446903321   |
| Autore                  | Zatt Bruno  |
| Titolo                  | 3D video coding for embedded devices : energy efficient algorithms and architectures // Bruno Zatt ...[et. al.]   |
| Pubbl/distr/stampa      | New York, : Springer Science, 2013  |
| ISBN                    | 1-4614-6759-4   |
| Edizione                | [1st ed. 2013.]   |
| Descrizione fisica      | 1 online resource (219 p.)  |
| Disciplina              | 004.1<br>006.22<br>620<br>621.381   |
| Soggetti                | Video compression<br>Digital video  |
| Lingua di pubblicazione | Inglese   |
| Formato                 | Materiale a stampa  |
| Livello bibliografico   | Monografia  |
| Note generali           | Description based upon print version of record.   |
| Nota di bibliografia    | Includes bibliographical references and index.  |
| Nota di contenuto       | Introduction -- Background and Related Work -- Multiview Video Coding Analysis for Energy and Quality -- Energy-Efficient Algorithms for Multiview Video Coding -- Energy-Efficient Architectures for Multiview Video Coding -- Results and Comparison -- Conclusion and future Works.  |
| Sommario/riassunto      | This book shows readers how to develop energy-efficient algorithms and hardware architectures to enable high-definition 3D video coding on resource-constrained embedded devices. Users of the Multiview Video Coding (MVC) standard face the challenge of exploiting its 3D video-specific coding tools for increasing compression efficiency at the cost of increasing computational complexity and, consequently, the energy consumption. This book enables readers to reduce the multiview video coding energy consumption through jointly considering the algorithmic and architectural levels. Coverage includes an introduction to 3D videos and an extensive discussion of the current state-of-the-art of 3D video coding, as well as energy-efficient algorithms for 3D video coding and energy-efficient hardware architecture for 3D video coding. . Discusses challenges related to performance and power in 3D video coding for embedded devices; |

- Describes energy-efficient algorithms for reducing computational complexity at multiple hierarchical levels;
  - Presents energy-efficient hardware architectures along with methods for reducing on-chip and off-chip energy related to both data processing and memory access;
  - Shows how to leverage jointly the algorithm and hardware architecture layers of the system.
-