Record Nr. UNINA9910736029603321 Autore Han Donghyeon **Titolo** On-Chip Training NPU - Algorithm, Architecture and SoC Design [[electronic resource] /] / by Donghyeon Han, Hoi-Jun Yoo Cham:,: Springer Nature Switzerland:,: Imprint: Springer,, 2023 Pubbl/distr/stampa **ISBN** 3-031-34237-2 Edizione [1st ed. 2023.] 1 online resource (249 pages) Descrizione fisica Altri autori (Persone) YooHoi-Jun Disciplina 621.3815 Soggetti Electronic circuits Embedded computer systems Microprocessors Computer architecture **Electronic Circuits and Systems Embedded Systems Processor Architectures** Lingua di pubblicazione Inglese **Formato** Materiale a stampa Livello bibliografico Monografia Chapter 1 Introduction -- Chapter 2 A Theoretical Study on Artificial Nota di contenuto Intelligence Training -- Chapter 3 New Algorithm 1: Binary Direct Feedback Alignment for Fully-Connected layer -- Chapter 4 New Algorithm 2: Extension of Direct Feedback Alignment to Convolutional Recurrent Neural Network -- Chapter 5 DF-LNPU: A Pipelined Direct Feedback Alignment based Deep Neural Network Learning Processor for Fast Online Learning -- Chapter 6 HNPU-V1: An Adaptive DNN Training Processor Utilizing Stochastic Dynamic Fixed-point and Active Bitprecision Searching -- Chapter 7 HNPU-V2: An Energy-efficient DNN Training Processor for Robust Object Detection with Real-World Environmental Adaptation -- Chapter 8 An Overview of Energy-efficient DNN Training Processors -- Chapter 9 Conclusion. Unlike most available sources that focus on deep neural network (DNN) Sommario/riassunto inference, this book provides readers with a single-source reference on the needs, requirements, and challenges involved with on-device, DNN training semiconductor and SoC design. The authors include coverage

of the trends and history surrounding the development of on-device

DNN training, as well as on-device training semiconductors and SoC design examples to facilitate understanding. Focuses on the requirements and challenges of on-device deep neural network (DNN) training, rather than DNN inference; Provides guidelines for on-device, DNN training semiconductor or System-on-Chip (SoC) design; Includes on-device training semiconductors and SoC design examples to facilitate understanding.