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	Sommario/riassunto	During the development of digital circuits, their functional correctness has to be ensured, for which formal verification methods have been established. However, the verification process using formal methods can have an exponential time or space complexity, causing the verification to fail. While exponential in general, recently it has been proven that the verification complexity of several circuits is polynomially bounded. Martha Schnieber proves the polynomial verifiability of several approximate circuits, which are beneficial in error-tolerant applications, where the circuit approximates the exact function in some cases, while having a lower delay or being more area-efficient. Here, upper bounds for the BDD size and the time and space complexity are provided for the verification of general approximate functions and several state-of-the-art approximate adders. About the author Martha Schnieber is working as a research assistant in the Group