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Sommario/riassunto

This book describes the first comprehensive approach to the optimization of interconnect architectures in 3D systems on chips (SoCs), specially addressing the challenges and opportunities arising from heterogeneous integration. Readers learn about the physical implications of using heterogeneous 3D technologies for SoC integration, while also learning to maximize the 3D-technology gains, through a physical-effect-aware architecture design. The book provides a deep theoretical background covering all abstraction-levels needed to research and architect tomorrow’s 3D-integrated circuits, an extensive set of optimization methods (for power, performance, area, and yield), as well as an open-source optimization and simulation framework for fast exploration of novel designs. Addresses modeling and optimization of (heterogenous) 3D interconnect architectures from

the physical to system level; Provides several optimization techniques for all key 3D-interconnect metrics; Presents the only open-source NoC simulator for heterogenous 3D SoCs.