

1. Record Nr.	UNINA9910710207403321
Autore	Fink J. L
Titolo	Corrosion evaluation of underground telephone cable shielding materials // J. L. Fink; E. Escalante
Pubbl/distr/stampa	Gaithersburg, MD : , : U.S. Dept. of Commerce, National Institute of Standards and Technology, , 1983
Descrizione fisica	1 online resource
Collana	NBSIR ; ; 83-2702
Altri autori (Persone)	FinkJ. L
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	1983. Contributed record: Metadata reviewed, not verified. Some fields updated by batch processes. Title from PDF title page.
Nota di bibliografia	Includes bibliographical references.

2. Record Nr.	UNINA9910483991003321
Titolo	Languages and Compilers for High Performance Computing : 17th International Workshop, LCPC 2004, West Lafayette, IN, USA, September 22-24, 2004, Revised Selected Papers // edited by Rudolf Eigenmann, Zhiyuan Li, Samuel P. Midkiff
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2005
Edizione	[1st ed. 2005.]
Descrizione fisica	1 online resource (X, 494 pages)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 3602
Altri autori (Persone)	EigenmannRudolf LiZhiyuan <1954-> MidkiffSamuel P <1954-> (Samuel Pratt)
Disciplina	004/.35
Soggetti	Compilers (Computer programs) Computer programming Computer science Computer networks Computer arithmetic and logic units Artificial intelligence - Data processing Compilers and Interpreters Programming Techniques Theory of Computation Computer Communication Networks Arithmetic and Logic Structures Data Science
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographic references and index.
Nota di contenuto	Experiences in Using Cetus for Source-to-Source Transformations -- The LLVM Compiler Framework and Infrastructure Tutorial -- An Overview of the Open Research Compiler -- Trimaran: An Infrastructure for Research in Instruction-Level Parallelism -- Phase-Based Miss Rate Prediction Across Program Inputs -- Speculative Subword Register Allocation in Embedded Processors -- Empirical Performance-Model

Driven Data Layout Optimization -- Implementation of Parallel Numerical Algorithms Using Hierarchically Tiled Arrays -- A Geometric Approach for Partitioning N-Dimensional Non-rectangular Iteration Spaces -- JuliusC: A Practical Approach for the Analysis of Divide-and-Conquer Algorithms -- Exploiting Parallelism in Memory Operations for Code Optimization -- An ILP-Based Approach to Locality Optimization -- A Code Isolator: Isolating Code Fragments from Large Programs -- The Use of Traces for Inlining in Java Programs -- A Practical MHP Information Analysis for Concurrent Java Programs -- Efficient Computation of Communicator Variables for Programs with Unstructured Parallelism -- Compiling High-Level Languages for Vector Architectures -- HiLO: High Level Optimization of FFTs -- Applying Loop Optimizations to Object-Oriented Abstractions Through General Classification of Array Semantics -- MSA: Multiphase Specifically Shared Arrays -- Supporting SQL-3 Aggregations on Grid-Based Data Repositories -- Supporting XML Based High-Level Abstractions on HDF5 Datasets: A Case Study in Automatic Data Virtualization -- Performance of OSCAR Multigrain Parallelizing Compiler on SMP Servers -- Experiences with Co-array Fortran on Hardware Shared Memory Platforms -- Experiments with Auto-Parallelizing SPEC2000FP Benchmarks -- An Offline Approach for Whole-Program Paths Analysis Using Suffix Arrays -- Automatic Parallelization Using the Value Evolution Graph -- A New Dependence Test Based on Shape Analysis for Pointer-Based Codes -- Partial Value Number Redundancy Elimination -- Overflow Controlled SIMD Arithmetic -- Branch Strategies to Optimize Decision Trees for Wide-Issue Architectures -- Extending the Applicability of Scalar Replacement to Multiple Induction Variables -- Power-Aware Scheduling for Parallel Security Processors with Analytical Models.
