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	Autore	Leibson Steve
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Architectural Basics; 3.1 Introduction to Configurable Processor Architectures; 3.2 Xtensa Registers; 3.3 Register Windowing; 3.4 The Xtensa Program Counter; 3.5 Memory Address Space; 3.6 Bit and Byte Ordering; 3.7 Base Xtensa Instructions; 3.8 Benchmarking the Xtensa Core ISA; Bibliography; 4 Basic Processor Configurability; 4.1 Processor Generation; 4.2 Xtensa Processor Block Diagram; 4.3 Pre-Configured Processor Cores; 4.4 Basics of TIE; 4.5 TIE Instructions; 4.6 Improving Application Performance Using TIE
4.7 TIE Registers and Register Files4.8 TIE Ports; 4.9 TIE Queue Interfaces; 4.10 Combining Instruction Extensions with Queues; 4.11 Diamond Standard Series Processor Cores-Dealing with Complexity; Bibliography; 5 MPSOC System Architectures and Design Tools; 5.1 SOC Architectural Evolution; 5.2 The Consequences of Architectural Evolution; 5.3 Memory Interfaces; 5.4 Memory Caches; 5.5 Local ROM and Local RAM Interfaces, the XLMI Port, and the PIF; 5.6 The PIF; 5.7 Ports and Queue Interfaces; 5.8 SOC Connection Topologies; 5.9 Shared-Memory Topologies; 5.10 Direct Port-Connected Topologies
5.11 Queue-Based System Topologies5.12 Existing Design Tools for Complex SOC Designs; 5.13 MPSOC Architectural-Design Tools; 5.14 Platform Design; 5.15 An MPSOC-Design Tool; 5.16 MPSOC System-Level Simulation Example; 5.17 SOC Design in the 21st Century; Bibliography; 6 Introduction to Diamond Standard Series Processor Cores; 6.1 The Diamond Standard Series of 32-bit Processor Cores; 6.2 Diamond Standard Series Software-Development Tools; 6.3 Diamond Standard Series Feature Summary; 6.4 Diamond Standard Series Processor Core Hardware Overview and Comparison
6.5 Diamond-Core Local-Memory Interfaces

Sommario/riassunto

Microprocessor cores used for SOC design are the direct descendents of Intel's original 4004 microprocessor. Just as packaged microprocessor ICs vary widely in their attributes, so do microprocessors packaged as IP cores. However, SOC designers still compare and select processor cores the way they previously compared and selected packaged microprocessor ICs. The big problem with this selection method is that it assumes that the laws of the microprocessor universe have remained unchanged for decades. This assumption is no longer valid.Processor cores for SOC designs can be far more plas

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