

1. Record Nr.	UNINA9910687994503321
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Titolo	Network-on-Chip : Architecture, Optimization, and Design Explorations // Isiaka A. Alimi [and three others]
Pubbl/distr/stampa	London : , : IntechOpen, , 2022
Descrizione fisica	1 online resource (110 pages) : illustrations
Disciplina	621.381531
Soggetti	Networks on a chip
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Sommario/riassunto	Limitations of bus-based interconnections related to scalability, latency, bandwidth, and power consumption for supporting the related huge number of on-chip resources result in a communication bottleneck. These challenges can be efficiently addressed with the implementation of a network-on-chip (NoC) system. This book gives a detailed analysis of various on-chip communication architectures and covers different areas of NoCs such as potentials, architecture, technical challenges, optimization, design explorations, and research directions. In addition, it discusses current and future trends that could make an impactful and meaningful contribution to the research and design of on-chip communications and NoC systems.