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| Nota di contenuto | Introduction -- Analog-to-Digital Conversion Fundamentals -- Architectural Considerations for High-Efficiency GHz-Range ADCs -- Ultrahigh-Speed High-Sensitivity Dynamic Comparator -- High-Speed Wide-Bandwidth Single-Channel SAR ADC -- High-Resolution Wide-Bandwidth Time-Interleaved RF ADC -- Ultra-Wideband Direct RF Receiver Analog Front End -- Conclusions, Contributions, and Future Work. . |
| Sommario/riassunto | This book proposes innovative circuit, architecture, and system solutions in deep-scaled CMOS and FinFET technologies, which address the challenges in maximizing the accuracy*speed/power of multi-GHz sample rate and bandwidth Analog-to-Digital Converters (ADC)s. A new holistic approach is introduced that first identifies the major error sources of a converter' building blocks, and quantitatively analyzes their impact on the overall performance, establishing the fundamental circuit-imposed accuracy – speed – power limits. The analysis extends |

to the architecture level, by introducing a mathematical framework to estimate and compare the accuracy – speed – power limits of several ADC architectures and variants. To gain system-level insight, time-interleaving is covered in detail, and a framework is also introduced to compare key metrics of interleaver architectures quantitatively. The impact of technology is also considered by adding process effects from several deep-scaled CMOS technologies. The validity of the introduced analytical approach and the feasibility of the proposed concepts are demonstrated by four silicon prototype Integrated Circuits (IC)s, realized in ultra-deep-scaled CMOS and FinFET technologies. Introduces a new, holistic approach for the analysis and design of high-performance ADCs in deep-scaled CMOS technologies, from theoretical concepts to silicon bring-up and verification; Describes novel methods and techniques to push the accuracy – speed – power boundaries of multi-GHz ADCs, analyzing core and peripheral circuits' trade-offs across the entire ADC chain; Supports the introduced analysis and design concepts by four state-of-the-art silicon prototype ICs, implemented in 28nm bulk CMOS and 16nm FinFET technologies; Provides a useful reference and a valuable tool for beginners as well as experienced ADC design engineers.