1. Record Nr. UNINA990007773170403321

Autore	Beatson, Jack
Titolo	Good faith and fault in contract law / Jack Beatson, Daniel Friedmann
Pubbl/distr/stampa	Oxford : Clarendon, 1995
Descrizione fisica	529 p. ; 24 cm
Disciplina	346.02
Locazione	DDCP
Collocazione	16-AB-170
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9910637722203321

Titolo	Machine Learning Applications in Electronic Design Automation / / edited by Haoxing Ren, Jiang Hu
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2022
ISBN	3-031-13074-X
Edizione	[1st ed. 2022.]
Descrizione fisica	1 online resource (585 pages)
Collana	Mathematics and Statistics Series
Disciplina	929.374 621.38150285631
Soggetti	Electronic circuits Embedded computer systems Electronic circuit design Electronic Circuits and Systems Embedded Systems Electronics Design and Verification
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia

Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Analysis of Digital Design: Routability Optimization for Industrial Designs at Sub-14nm Process Nodes Using Machine Learning -- RouteNet: Routability Prediction for Mixed-size Designs Using Convolutional Neural Network -- High Performance Graph Convolutional networks with Applications in Testability Analysis -- MAVIREC: ML-Aided Vectored IR-Drop Estimation and Classification -- GRANNITE: Graph Neural Network Inference for Transferable Power Estimation -- Machine Learning-Enabled High-Frequency Low-Power Digital Design Implementation at Advanced Process Nodes -- Optimization of Digital Design: Chip Placement with Deep Reinforcement learning -- DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement -- TreeNet: Deep Point Cloud Embedding for Routing Tree Construction -- Asynchronous Reinforcement Learning Framework for Net Order Exploration in Detailed Routing -- Standard Cell Routing with Reinforcement Learning and Genetic Algorithm in Advanced Technology Nodes -- PrefixRL: Optimization of Parallel Prefix Circuits using Deep Reinforcement Learning -- GAN-CTS: A Generative Adversarial Framework for Clock Tree Prediction and Optimization -- Analysis and Optimization of Analog Design: Machine Learning Techniques in Analog Layout Automation -- Layout Symmetry Annotation for Analog Circuits with Graph Neural Networks -- ParaGraph: Layout parasitics and device parameter prediction using graph neural network -- GCN-RL circuit designer: Transferable transistor sizing with graph neural networks and reinforcement learn -- Parasitic-Aware Analog Circuit Sizing with Graph Neural Networks and Bayesian Optimization -- Logic and Physical Verification: Deep Predictive Coverage Collection/ Dynamically Optimized Test Generation Using Machine Learning -- Novelty-Driven Verification: Using Machine Learning to Identify Novel Stimuli and Close Coverage -- Using Machine Learning Clustering To Find Large Coverage Holes -- GAN-OPC: Mask optimization with lithography-guided generative adversarial nets -- Layout hotspot detection with feature tensor generation and deep biased learning.
Sommario/riassunto	This book serves as a single-source reference to key machine learning (ML) applications and methods in digital and analog design and verification. Experts from academia and industry cover a wide range of the latest research on ML applications in electronic design automation (EDA), including analysis and optimization of digital design, analysis and optimization of analog design, as well as functional verification, FPGA and system level designs, design for manufacturing (DFM), and design space exploration. The authors also cover key ML methods such as classical ML, deep learning models such as convolutional neural networks (CNNs), graph neural networks (GNNs), generative adversarial networks (GANs) and optimization methods such as reinforcement learning (RL) and Bayesian optimization (BO). All of these topics are valuable to chip designers and EDA developers and researchers working in digital and analog designs and verification. Serves as a single-source reference to key machine learning (ML) applications and methods in digital and analog design and verification; Covers classical ML methods, as well as deep learning models such as convolutional neural networks (CNNs), graph neural networks (GNNs), generative adversarial networks (GANs) and optimization methods such as reinforcement learning (RL) and Bayesian optimization (BO); Discusses machine learning ML's applications in electronic design automation (EDA), especially in the design automation of VLSI integrated circuits.