Record Nr.	UNINA9910631096403321
Autore	Raji Mohsen
Titolo	Lifetime reliability-aware design of integrated circuits / / Mohsen Raji, Behnam Ghavami
Pubbl/distr/stampa	Cham, Switzerland : , : Springer, , [2023] ©2023
ISBN	3-031-15345-6
Descrizione fisica	1 online resource (113 pages)
Disciplina	354.81150006
Soggetti	Integrated circuits - Reliability
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Intro Preface Acknowledgment Contents Impacts of Process Variations and Aging on Lifetime Reliability of Flip-Flops 1 Introduction 2 Analysis Methodology 2.1 Flip-Flop Topologies Under Study 2.2 Timing Parameters of Flip-Flops 2.3 Aging Effects 2.4 BTI Model 2.5 Process Variation Model 3 Vth Degradation Analysis Approach 4 Timing Yield-Aware Lifetime Reliability Metric 5 Experimental Results 5.1 Characterization Setup 5.2 FF Characterization Results 5.3 Aging Impacts on Lifetime Reliability 5.4 Power-Delay-Product Comparison of FFs 6 Discussion and Conclusions References Restructuring-Based Lifetime Reliability Improvement of Nanoscale Master-Slave Flip-Flops 1 Introduction 2 Proposed Lifetime Reliability Improvement Approach 2.1 Basic Idea 2.2 Technique Application to TGFF 2.3 Technique Application to TGFFV2 2.4 Technique Application to WPMS 2.5 Technique Application to C2MOS 2.6 Transistor Sizing 3 Experimental Results 3.1 Characterization Setup 3.2 Lifetime Reliability Increase 3.3 Cost Evaluation 4 Conclusion References Lifetime Reliability Improvement of Pulsed Flip-Flops 1 Introduction 2 Proposed Lifetime Improvement Approach 2.1 Basic Idea 2.2 Application of the Technique to HLFF 2.3 Application of the Technique to SDFF 2.4 Application of Technique to USDFF 2.5 Technique Application to XCFF 3 Experimental Results 3.1 Characterization Setup 3.2 FF Characterization

1.

Results -- 3.3 Lifetime Reliability of Both Structures -- 3.4 Lifetime Reliability Increase -- 3.5 Cost Evaluation -- 4 Conclusion --References -- Gate Sizing-Based Lifetime Reliability Improvement of Integrated Circuits -- 1 Introduction -- 2 Proposed Framework -- 2.1 Statistical Gate Delay Model Under the Joint Effects of NBTI and PV. 2.1.1 Initial Gate Delay Under PV Effects -- 2.1.2 Delay Degradation Under the Joint Effects of NBTI and PV Considering Spatial Correlation -- 2.2 Statistical Circuit-Level Delay Computation Considering the Joint Effects of NBTI and PV -- 2.2.1 Arrival Time Propagation -- 2.2.2 Merging Arrival Times -- 2.3 Incremental Criticality-Based Statistical Gate-Sizing Algorithm -- 3 Experimental Results -- 3.1 Circuit Lifetime Reliability Optimization -- 4 Conclusion -- References -- Joint Timing Yield and Lifetime Reliability Optimization of Integrated Circuits -- 1 Introduction -- 2 Problem Formulation -- 3 Gate-Level Delay Model Under the Joint Effects of NBTI and PV -- 3.1 Initial Gate Delay Under PV -- 3.2 Delay Degradation Under Joint Effects of NBTI and PV -- 4 Gate Sizing Method -- 4.1 First Phase: Initial Delay Optimization -- 4.2 Second Phase: Guardband Optimization -- 4.2.1 Guiding Metrics --4.2.2 Multiobjective Ranking -- 5 Experimental Results -- 5.1 Effect of Timing Yield Optimization -- 5.2 Evaluation of the Delay Degradation-Aware Gate Criticality Metric -- 6 Conclusion -- References -- Lifetime Reliability Optimization Algorithms of Integrated Circuits Using Dual-Threshold Voltage Assignment -- 1 Introduction -- 2 PV- and BTI-Aware Gate Delay Model -- 3 Guardband-Aware Lifetime Reliability (GAR) Metric -- 4 Dual-Threshold Voltage Assignment Technique --4.1 Motivation Example -- 4.2 Vth Assignment Technique Overhead --5 Lifetime Reliability Optimization Flow -- 5.1 Process Variation- and BTI-Aware Criticality Metric -- 5.2 Optimization Algorithm-Based DVth Assignment Policy -- 5.2.1 Optimization Approach #1: Greedy-Based Method (GeRO) -- 5.2.2 Optimization Approach #2: Simulated-Annealing-Based Method (SARO) -- 5.2.3 Optimization Approach #3: Sensitivity-Based Method (TIRO) -- 6 Experimental Results. 6.1 PV- and BTI-Aware Delay Degradation Model Verification -- 6.2 Lifetime Reliability Analysis -- 6.3 Lifetime Reliability Optimization --6.4 Algorithm Computation Complexity and Runtime -- 7 Conclusion -- References -- Index.