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Nota di contenuto	Intro -- Preface -- Organization -- Contents -- 100% Visibility at MHz Speed: Efficient Soft Scan-Chain Insertion on AMD/Xilinx FPGAs -- 1 Introduction -- 1.1 Related Work -- 2 Background -- 3 Soft Scan-Chain Methodology -- 4 Experimental Results -- References -- FPGA-Accelerated Tersoff Multi-body Potential for Molecular Dynamics Simulations -- 1 Introduction -- 2 Background -- 2.1 Classical MD with Tersoff Potential -- 2.2 Prior MD Work -- 3 Efficient Data Transfer -- 3.1 Bandwidth-Friendly Particle Mapping -- 3.2 Zigzagging Buffer Design -- 4 Fixed-Point Design -- 4.1 Dynamic Range Analysis -- 4.2 Precision Analysis -- 5 Custom Dataflow Design -- 6 Evaluation -- 6.1 Environment Setup -- 6.2 Evaluation Performance -- 6.3 Resource Usage Evaluation -- 6.4 Energy Evaluation -- 7 Conclusion -- References -- A Runtime Programmable Accelerator for Convolutional and Multilayer Perceptron Neural Networks on FPGA -- 1 Introduction -- 2 CNN-MLPA Architecture -- 2.1 Processing Element -- 2.2 Scheduler -- 2.3 Controller -- 2.4 Configuration Registers -- 3 Evaluation and Results for MLP Operations -- 3.1 Test Platform -- 3.2 CNN-MLPA Configurations -- 3.3 Test Applications -- 3.4 Performance Evaluation of MLP Accelerator -- 3.5 Resource Utilization and Performance Comparison with Other Works -- 4 Accelerator with CNN Feature -- 4.1 Results for Full CNN-MLP Acceleration -- 5 Conclusion

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