

1. Record Nr.	UNINA9910555117603321
Autore	Tripathi Suman Lata
Titolo	Digital VLSI design and simulation with Verilog // Suman Lata Tripathi [et al.]
Pubbl/distr/stampa	Hoboken, NJ : , : John Wiley & Sons, Inc., , [2022] ©2022
ISBN	1-119-77808-5 1-119-77809-3 1-119-77806-9
Descrizione fisica	1 online resource (222 pages)
Disciplina	621.395028553
Soggetti	Integrated circuits - Very large scale integration - Design and construction Verilog (Computer hardware description language) Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Sommario/riassunto	The integrated circuits are now growing its importance in every electronic system that needs an efficient VLSI architecture designs with low power consumption, compress chip area, speed, and operating frequency. The challenge for VLSI system designers is to optimize the hardware-software integration for lowering the total cost of acquisition of products. So, there is a demand for better technological solutions for advanced VLSI architectures that can be done through hardware description language (HDL). Verilog HDL is one of the programming languages that can give better solutions to this new era of the VLSI industry.