1. Record Nr. UNINA9910544876503321

Titolo	A combined data and power management infrastructure : for small satellites / / Jens Eickhoff, editor
Pubbl/distr/stampa	Berlin, Germany : , : Springer, , [2021] ©2021
ISBN	9783662640531 9783662640524
Edizione	[Second edition.]
Descrizione fisica	1 online resource (459 pages)
Collana	Springer aerospace technology
Disciplina	629.46
Soggetti	Artificial satellites - Control systems Artificial satellites - Electronic equipment
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Intro -- Foreword by Robin Biesbroek -- Foreword by Ana Ambrosio -- Foreword by Olivier L. de Weck -- Foreword by René Laufer -- Foreword by Peter Martinez -- Preface -- Donation for Life -- Contents -- List of Abbreviations -- 1 System Design Concept -- 1.1 Introduction -- 1.2 The Onboard Computer Concept -- 1.3 The PCDU with Enhanced Functionality -- 1.4 CPU-Board Reconfiguration Control -- 1.4.1 Component Functions During Failure Handling -- 1.4.2 A Combined Controller for PCDU and CPU FDIR -- 1.4.3 Failure Management with the Combined-Controller -- 1.4.4 Advantages of the Combined-Controller Approach -- 1.5 CDPI Software Functions -- 1.5.1 Software Initialization -- 1.5.2 SpaceWire Network Initialization and FDIR -- 1.5.3 Remote-Board Reconfiguration Management -- 1.6 Firmware Functions -- 1.6.1 Pulse per Second Signal Management -- 1.6.2 I/O-Board Interface Operation and Group Tailoring -- 1.6.3 Ground/Space Communication -- 1.7 Board Identification -- 1.8 Completeness of System Architecture -- 1.9 Outlook for Future Missions -- 2 OBC CPU-Boards -- 2.1 Introduction -- 2.2 GR712RC-SBC -- 2.2.1 Board Block Diagram -- 2.2.2 Processor -- 2.2.3 Memory -- 2.2.4 Interface Circuits -- 2.2.5 Auxiliary Circuits -- 2.2.6 Mechanical Layout and Constraints -- 2.2.7 PCB Design and Constraints -- 2.2.8 Housing and Connectors -- 2.2.9

Components -- 3 OBC Periphery Boards -- 3.1 Common Design for SpaceWire Routers, I/O and CCSDS-Boards -- 3.2 OBC Periphery Boards Overview -- 3.3 FPGA-Mezzanine -- 3.3.1 FPGA -- 3.3.2 Memory -- 3.3.3 FPGA Configuration -- 3.4 Carrier -- 3.4.1 JTAG -- 3.4.2 Configurable IO -- 3.4.3 SpaceWire -- 3.4.4 Ethernet -- 3.5 System Architecture -- 3.5.1 Board Implementation -- 3.5.2 System Grounding -- 3.5.3 Power Budget -- 3.5.4 Physical Structure -- 3.5.5 Loki-Board IO Connectors -- 3.5.6 Loki-Board Radiation Characteristic. 3.5.7 Loki-Board Temperature Limits -- 4 SpaceWire Router Boards -- 4.1 SpaceWire Routers for Ground and Flight -- 4.2 General Router Functions -- 4.3 Router Board Structure -- 4.4 Peripherals -- 4.4.1 Peripheral Identification &amp -- Configuration (PID) -- 4.4.2 Memory and Applications -- 4.4.3 SpaceWire Ports -- 4.4.4 SpaceWire-Ethernet Bridge -- 4.4.5 FPGA Resources -- 4.4.6 Configuration -- 4.4.7 PPS Interfaces -- 4.5 Router-Board Programmers Model -- 4.5.1 RMAP0 -- 4.5.2 Router Configuration Space -- 4.5.3 Port0 RMAP SpaceWire Codec -- 4.5.4 Port0 RMAP PPS -- 4.5.5 MRAM -- 4.5.6 Ethernet -- 5 I/O-Boards -- 5.1 General I/O-Board Functions -- 5.2 I/O Board Structure -- 5.3 Memory and Applications -- 5.4 Peripherals -- 5.4.1 I/O-Board Internal Router -- 5.4.2 SpaceWire Ports -- 5.4.3 UART Interfaces -- 5.4.4 GPIO Interfaces -- 5.5 I/O Board Programmers Model -- 5.5.1 RMAP0 -- 5.5.2 Router Configuration Space -- 5.5.3 SpaceWire Codec -- 5.5.4 MRAM -- 5.5.5 Configurable I/O Interfaces -- 5.5.6 UART -- 5.5.7 GPIO -- 6 CCSDS Decoder/Encoder Boards -- 6.1 Introduction -- 6.2 CCSDS-Board Hardware -- 6.2.1 Onboard Memory -- 6.2.2 Peripherals -- 6.2.3 Memory -- 6.2.4 FPGA Resources -- 6.2.5 Configuration -- 6.3 Functional Overview -- 6.3.1 Interfaces -- 6.3.2 Command Link Control Word Coupling -- 6.3.3 Clock and Reset -- 6.3.4 Performance -- 6.3.5 Error Mitigating Strategy -- 6.3.6 SpaceWire Link Interfaces -- 6.3.7 On-Chip Memory -- 6.3.8 Signal Overview -- 6.3.9 Telemetry Encoder Functional Overview -- 6.3.10 Telecommand Decoder Functional Overview -- 6.4 Telemetry Encoder -- 6.4.1 Layers -- 6.4.2 Data Link Protocol Sub-layer -- 6.4.3 Synchronization and Channel Coding Sub-layer -- 6.4.4 Physical Layer -- 6.4.5 Connectivity -- 6.4.6 Operation -- 6.4.7 Registers -- 6.4.8 Signal Definitions and Reset Values -- 6.4.9 TM Encoder-Virtual Channel Generation.
6.4.10 TM Encoder-Descriptor -- 6.4.11 TM Encoder-Virtual Channel Generation Function Input Interface -- 6.5 TC Decoder-Flight Software Commands -- 6.5.1 Overview -- 6.5.2 Waveforms -- 6.5.3 Coding Layer (CL) -- 6.5.4 Transmission -- 6.5.5 Relationship Between Buffers and FIFOs -- 6.5.6 Command Link Control Word Interface (CLCW) -- 6.5.7 Configuration Interface (AMBA AHB Slave) -- 6.5.8 Interrupts -- 6.5.9 Registers -- 6.5.10 Signal Definitions and Reset Values -- 6.6 TC Decoder-High Priority Commands -- 6.6.1 Overview -- 6.6.2 Operation -- 6.6.3 Telecommand Transfer Frame Format-Hardware Commands -- 6.6.4 Signal Definitions and Reset Values -- 6.7 SpaceWire Interface with RMAP Target -- 6.8 JTAG Debug Interface -- 6.9 Diverse Features -- 6.10 CCSDS Processor Spacecraft Specific Configuration -- 7 Integrated Mass Memory Unit -- 7.1 General -- 7.2 Introduction -- 7.3 System Overview with Peripherals -- 7.4 Mass Memory Handling -- 7.4.1 Partition Configuration -- 7.4.2 Memory Recovery -- 7.4.3 SpaceWire RMAP Implementation -- 7.5 Memory Mapping -- 7.6 Interrupt Sources -- 7.7 Electrical Characteristics -- 7.7.1 Connectors -- 7.7.2 Power Consumption -- 7.8 Mechanical Characteristics -- 7.9 Radiation Hardness Characteristics -- 8 OBC Module and Cassette Concept -- 8.1 OBC-Housing Basics -- 8.1.1 The Different Boards of the OBC -- 8.1.2 Concept of the Cassettes -- 8.1.3 The OBC

as Stacked Cassettes -- 8.1.4 Mount Points of the OBC -- 8.1.5 Internal Harness Basics -- 8.2 Mechanical Design of the Cassettes -- 8.2.1 Design Concept -- 8.2.2 Individual Cassette Design -- 8.3 Summary -- 9 OBC Internal Harness -- 9.1 Internal Harness Overview -- 9.1.1 The SpaceWire Harness -- 9.1.2 The Power Harness -- 9.1.3 CLCW Interconnects -- 9.1.4 Pulse Line Connections -- 9.1.5 JTAG Interfaces -- 9.1.6 Crypto-Key Load Interfaces -- 9.2 Interfaces Per OBC Subunit. 9.3 Remote Board Nominal/Redundant Identification -- 10 Board Interconnects to Cassettes -- 10.1 Introduction -- 10.2 Flex-PCBs Model to Market -- 10.3 Router-Board Flex in Detail -- 10.4 I/O-Cassette Flex Overview -- 10.5 CCSDS-Cassette Flex Overview -- 11 Modular Power-Boards -- 11.1 Introduction -- 11.2 Mechanical Concept -- 11.3 Electrical Concept -- 11.4 Thermal Concept -- 11.5 The DC/DC Converters -- 11.5.1 VPT Main Converter -- 11.5.2 Intersil Converter -- 11.6 MPB Combined Efficiency -- 11.7 PCB Layout -- 11.8 MPB Schematic Design -- 11.9 MPB Variants -- 12 OBC Thermal Analysis -- 12.1 Introduction -- 12.1.1 Geometrical Mathematical Model of the Housing -- 12.1.2 Dissipation Points: Router Board -- 12.1.3 Dissipation Points: I/O-Board -- 12.1.4 Dissipation Points: CCSDS-Board -- 12.1.5 Dissipation Points: MMU and MPB -- 12.1.6 Dissipation Points: CPU-Board and MPB -- 12.1.7 Summary of Dissipation Values -- 12.2 Assumptions -- 12.2.1 Components -- 12.2.2 Environment -- 12.3 Results -- 12.3.1 Case 01 -- 12.3.2 Case 02 -- 12.4 OBC Housing Material Properties -- 13 Power Control and Distribution Unit -- 13.1 Introduction -- 13.2 The PCDU in a Typical Power Supply Subsystem -- 13.3 PCDU Unit Design Overview -- 13.3.1 PCDU Interfaces -- 13.3.2 PCDU Command Concept -- 13.4 Boot-Up Sequence of the PCDU and PCDU Modes -- 13.5 Power Control and Distribution Functions -- 13.6 PCDU Specific Functions in the CDPI Architecture -- 13.6.1 Analog Data Handling Concept -- 13.6.2 Reconfiguration Logic for the OBC -- 13.6.3 Reconfiguration Functionality for the Spacecraft -- 13.7 Diverse PCDU Functions -- 13.7.1 Launcher Separation Detection -- 13.7.2 Control and Monitoring of Solar Panel Deployment (Optional) -- 13.7.3 Control of the Payload Data Transmission Subsystem Power -- 13.7.4 History Log Function. 13.7.5 Time Synchronization Between Internal Controllers -- 13.7.6 Overvoltage Protection -- 13.8 PCDU Environmental Qualification Characteristics -- 13.8.1 Thermal-Vacuum Limits -- 13.8.2 Radiation Limits -- 13.8.3 Vibration Limits -- 13.9 List of Connectors -- 13.10 PCDU Commands Overview -- 13.11 The PCDU and Electric Propulsion Systems -- 14 CDPI Functional Testing -- 14.1 Introduction -- 14.2 Test Scope -- 14.3 Test Conditions -- 14.4 Test Plan, Test Procedures and Setups -- 14.4.1 Power-Board Tests -- 14.4.2 CPU-Board Tests -- 14.4.3 SpaceWire RTR-Board Tests -- 14.4.4 I/O-Boards Tests -- 14.4.5 CCSDS-Boards Tests -- 14.4.6 MMU Tests -- 14.4.7 PCDU Tests -- 14.4.8 OBC Subsystem Tests -- 14.4.9 CDPI Reconfiguration Tests -- 14.5 Test Execution on STB -- 14.5.1 Satellite Testbed Infrastructure -- 14.5.2 Typical Test Stages on a Satellite Testbed -- 14.6 Test Execution on FlatSat -- 15 OBC Mechanical Qualification -- 15.1 Introduction -- 15.2 Structural Analysis -- 15.3 Determination of Eigenfrequencies -- 15.4 Vibration Testing -- 15.5 Shock Testing -- 15.6 Mechanical Properties -- 16 Example Missions -- 16.1 ClearSpace "ADRIOS CS-1" -- 16.1.1 The Motivation -- 16.1.2 The ClearSpace-1 Service to ESA -- 16.1.3 The Target -- 16.1.4 The Mission -- 16.1.5 The ClearSpace-1 Servicer -- 16.2 Thailand Space Program and FLP2 -- 16.3 Stuttgart University "Flying Laptop" -- 16.3.1 Technology and Payloads -- 16.3.2 Satellite Attitude Control System -- 16.3.3 Satellite Electrical Architecture and Block Diagram -- 17 Annexes

and Data Sheets -- 17.1 GR712RC-SBC Interface Board -- 17.1.1 Power Circuits -- 17.1.2 JTAG (FTDI USB) Interface -- 17.1.3 Interface Configuration Logic/Circuits &amp -- GPIO/GPIN -- 17.1.4 Mechanical Layout, Design and Constraints -- 17.1.5 List of Connectors-IF-Board -- 17.1.6 List of Oscillators, Switches and LED's-IF-Board.
17.1.7 List of Switches and LED's-IF-Board.