

1. Record Nr.	UNINA9910544845303321
Autore	Belous A. I (Anatolii Ivanovich)
Titolo	The art and science of microelectronic circuit design // A. I. Belous, Vitali Saladukha
Pubbl/distr/stampa	Cham, Switzerland : , : Springer, , [2022] ©2022
ISBN	3-030-89854-7
Descrizione fisica	1 online resource (445 pages)
Disciplina	621.38173
Soggetti	Integrated circuits
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Intro -- Preface -- Acknowledgements -- Contents -- Chapter 1: Standard Characteristics of Digital Microcircuits -- 1.1 Structure of Digital Microcircuits -- 1.1.1 General Structure of Digital Microcircuits -- 1.1.2 Architecture of Internal Cells of Digital Microcircuits -- 1.1.3 Architecture of Digital Microcircuit Matching Elements -- 1.2 System of Main Parameters and Characteristics of Digital Microcircuits -- 1.2.1 Functional Parameters of Digital Microcircuits -- 1.2.2 Electrical Parameters of Digital Microcircuits -- 1.2.3 Dynamic Parameters of Digital Microcircuits -- 1.3 Schematic Implementation of Digital Microcircuits -- 1.3.1 Power Characteristics of Standard Logic Cells of Digital Microcircuits -- 1.3.2 Schematic Implementation of Standard Digital Microcircuits -- 1.3.3 Techniques of Digital Microcircuits Element Base Selection -- 1.4 Impact of Destabilizing Factors on Serviceability of Digital Microcircuits -- 1.4.1 Immunity of Digital Microcircuits to Electrostatic Discharge -- 1.4.2 Microcircuits Overload Tolerance -- 1.4.3 Dependence of Electrical Characteristics of Digital Microcircuits Upon Operational Modes -- 1.4.4 Immunity of Digital Microcircuits to the Impact Produced by Interferences -- 1.5 Parasitic Elements and Effects in Digital Microcircuits -- 1.5.1 Parasitic Transistor Elements Inside Digital Microcircuit Dice -- 1.5.2 Miller's Effect -- 1.5.3 Latch-Up Effect -- References -- Chapter 2: Schematic Solutions of Digital CMOS Microcircuits -- 2.1 Standard Logic Cells of Digital CMOS Microcircuits -- 2.1.1 Static CMOS Logic Cells -- 2.1.2

Standard LC of Dynamic CMOS Logic -- 2.2 Memory Elements of the Digital CMOS Integrated Circuits -- 2.2.1 Memory Elements, Clocked by the Level of the Synchrosignal -- 2.2.2 Memory Elements, Clocked by the Synchrosignal Edge -- References.

Chapter 3: Schematic Technical Solutions of the Bipolar Integrated Circuits -- 3.1 Digital Integrated Circuits on the Bipolar Transistors with the Schottky Diodes -- 3.1.1 Basic TTLS Logic Elements of Digital Integrated Circuits -- 3.1.2 Basic Logic Elements of Schottky Transistor Logic -- 3.1.3 Basic Logic Elements of the Integrated Schottky Logic -- 3.1.4 Base Logic Elements of the Diode-Transistor Logic with Schottky Diodes -- 3.2 Memory Elements of TTLS Integrated Circuits -- 3.2.1 Memory Elements, Synchrosignal Edge Cycled -- 3.2.2 Memory Elements, Cycled by the Level of the Synchrosignal -- 3.3 Schematics of the Input Matching Elements of the TTLS Integrated Circuits -- 3.3.1 Input Matching TTLS Elements of Integrated Circuits with the standard TTL input levels -- 3.3.2 Input ME TTLS of Integrated Circuits with the Enhanced Load Capacitance -- 3.3.3 Input ME TTLS of the Integrated Circuits with the Paraphrase Outputs -- 3.3.4 Input ME TTLS Integrated Circuits with Memory -- 3.3.5 Input BE TTLS of Integrated Circuits with the Enhanced Noise Immunity -- 3.3.6 Input Matching Element with Conversion of the Signal Levels -- 3.3.7 Protection Diagrams of the Input ME TTLS Integrated Circuits -- 3.4 Schematics of the Output Matching Elements of TTLS Integrated Circuits -- 3.4.1 Output ME TTLS of Integrated Circuits with Standard TTL Output Levels -- 3.4.2 Output ME of TTLS Integrated Circuits with Memory -- 3.4.3 Output ME of TTLS Integrated Circuits with Conversion of signal levels -- 3.4.4 Schematics of the Protection Circuits of the Output ME of TTLS Integrated Circuits -- 3.5 Digital Integrated Circuits on the Basis of the Integrated Injection Logic -- 3.5.1 Varieties of the Basic Elements of the I²L Integrated Circuits -- 3.5.2 Memory Elements of I²L Integrated Circuits. 3.5.3 Schematics of the Input Matching Elements of the I²L Integrated Circuits -- 3.5.4 Protection of the I²L Pins of the Integrated Circuits from Overvoltage and Static Electricity -- References -- Chapter 4: Circuit Engineering of Bi-CMOS IC -- 4.1 Basic Logic Elements of Bi-CMOS IC -- 4.2 Bi-CMOS IC Memory Elements -- 4.3 Circuit Engineering of Bi-CMOS IC Input Matching Components -- 4.3.1 Input MC of Bi-CMOS IC with Signal Level Conversion -- 4.3.2 Input MC of Bi-CMOS IC with Increased Load Capacity -- 4.3.3 Input MC of Bi-CMOS IC with Paraphrase Outputs -- 4.3.4 Input MC of Bi-CMOS IC with Increased Noise Immunity -- 4.3.5 Input MC of Bi-CMOS Memory IC -- 4.3.6 Circuit Engineering of Input MC of Bi-CMOS IC Protection -- 4.4 Circuit Engineering of Bi-CMOS IC Matching Output Components -- 4.4.1 Output MC of Bi-CMOS IC with the Formation of CMOS Output Levels -- 4.4.2 Output MC of Bi-CMOS ICs with the Formation of TTL Output Levels -- 4.4.3 Output MC of Bi-CMOS IC with the Formation of ECL Output Levels -- 4.4.4 Output MC Bi-CMOS Memory ICs -- 4.4.5 Circuit Engineering of the Output MC Bi-CMOS IC Protection Circuits -- References -- Chapter 5: Structure and Specific Features of Design Libraries for Submicron Microcircuits -- 5.1 Development Process Flow and Standard Structure of a Process Design Kit (PDK) -- 5.2 Terms and Definitions Used to Describe PDK Components -- 5.3 PDK Standardization -- 5.4 Mixed Analog/Digital Microcircuit Design Flow -- 5.5 Summarized Information Model of Mixed Analog-Digital IC Design -- 5.6 Specifying Basic PDK Components and Standard Elements List -- 5.7 Development Features of Digital Libraries for Designing ASICs with Submicron Design Rules -- 5.8 Structural and Circuit-Level Features of Designing Basic Cells for Submicron Microcircuits Library -- 5.8.1 Voltage Level Shifters -- 5.8.2 Power Gating Circuits.

5.8.3 Isolation Library Cells for Submicron Microcircuits -- 5.8.4
`Always-on` Buffers -- 5.9 Standard PDK Data Files -- 5.10
Standard PDK Current Source Models (CCS) -- 5.11 Methods and
Examples of Standard IC Design Tools Adaptation to 90, 65, and 45 Nm
Microcircuit Design -- 5.11.1 Synopsys Tutorial (Educational) Design
Kit: Capabilities, Applications, and Prospects -- 5.11.2 Synopsys EDK
Overview -- 5.11.3 Synopsys Digital Standard Cell Library -- 5.11.4 I/O
Standard Cell Library -- 5.11.5 Standard Set of PDK Memory Modules
-- 5.11.6 Phase-Locked Loop (PLL) -- 5.11.7 Geography of EDK
Applications and Prospects -- 5.12 Contents of Educational Design Kits
Provided by IMEC -- References -- Chapter 6: Digital IC and System-
on-Chip Design Flows -- 6.1 Choosing the IC Design Flow -- 6.2
System Design Stage -- 6.3 Functional Design Stage (Fig. 6.3) -- 6.4
Logic Design Stage -- 6.5 Physical (Topological) Design Stage -- 6.6
Stage of Physical Verification and Preparation for Production (Fig. 6.6)
-- 6.7 Project Certification -- 6.8 SoC Design Flow -- 6.8.1 Trends in
the Development of Design Tools -- 6.8.2 SoC Design Methodology --
6.8.3 SoC Design Flow -- 6.8.4 SoC System Design -- 6.8.5 CAD
Software for the System Level -- 6.9 Practical Example of the System-
on-Chip Simulation -- 6.9.1 Standard Design Flow of the SoC of
Cadence Company -- 6.9.2 Description of the Simulation and
Verification Environment -- 6.9.3 Project in the Cadence Incisive
Environment -- References -- Chapter 7: Fundamentals of CMOS
Microcircuits Logic Design with Reduced Power Consumption -- 7.1
Basics of Low-Power-Driven Logic Synthesis of CMOS Microcircuits --
7.2 Identification of Power Dissipation Sources in CMOS Microcircuits
-- 7.3 Probabilistic Evaluation of Optimization Options by Predicted
Switching Activity of IC Nodes.
7.4 Selection of Element Basis for Low-Power CMOS Microcircuit Design
-- 7.5 Logic Synthesis of CMOS Microcircuits in the Basis of Library
Elements -- 7.6 Power Dissipation-Driven Optimization of Two-Level
Logic Circuits -- 7.7 Selection of Basic Gates for Technology-
Independent Functional Circuit -- 7.8 Optimization of Multilevel Logic
Circuits of Multi-input Gates -- 7.9 Optimization of Multilevel Logic
Circuits of Double Input Gates -- 7.10 Technology Mapping -- 7.11
Estimation of Power Consumption of Designed CMOS Microcircuits at
Logic and Circuitry Levels -- 7.12 Low-Power CMOS Microcircuit Design
Technology with ELS Package -- 7.13 ELS Software Package
Architecture -- 7.14 Functional Capabilities of ELS Software Package --
References -- Chapter 8: Fundamentals of Building a Quality
Management System for Manufacturing Submicron Integrated Circuits
Based on Test ... -- 8.1 Methodology of the Organization of
Technological Test Control in the Process of Design and Production of
Microelectronic P... -- 8.1.1 Place and Role of Semiconductor Test
Structures in the Process of Manufacturing Integrated Circuits -- 8.1.2
Classification of Technological Test Structures -- 8.1.3 Methods of
Placing Test Structures on Semiconductor Wafers -- 8.2 Principles of
Control of the Process of Manufacturing Chips Using Test Structures --
8.2.1 Assessment of the Quality of the Process Based on the Method of
Interoperative Control of Wafers -- 8.2.2 Typical Composition of the
Test Module for Monitoring Production Processes -- 8.2.3 Typical
Composition of Test Structures for Quality Control of Submicron ICs --
8.2.4 Statistical Processing of Measurement Results of Test Structures
-- 8.3 Forecasting the IC Yield Based on the Results of the Test Control
-- 8.3.1 Features of Simulation of the IC Yield.
8.3.2 Model of Postoperative Separation of Defects in the Technological
Process of IC Manufacturing.
