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Sommario/riassunto	This book introduces power amplifier design in 22nm FDSOI CMOS dedicated towards 5G applications at 28 GHz and presents 4 state-of-the-art power amplifier designs. The authors discuss power amplifier performance metrics, design trade-offs, and presents different power amplifier classes utilizing efficiency enhancement techniques at 28 GHz. The book presents the design process from theory, simulation, layout, and finally measurement results. Covers thoroughly design steps starting from theory, to simulation, layout and measurement steps; Includes simulation details and comparison with existing state of the art designs; Shows not only the design of the power amplifier block, but also the steps taken to integrate it into a complete phased array transmitter architecture; Discusses design trade-offs at high

frequency, including performance metrics and technology limitations, and discusses different ways to overcome them.