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Nota di contenuto	Introduction -- CGRA background -- Concept of the Blocks architecture -- The Blocks framework -- Energy, area, and performance evaluation -- Architectural model -- Case study: the BrainSense platform -- Conclusion.
Sommario/riassunto	This book describes a new, coarse-grained reconfigurable architecture (CGRA), called Blocks, and puts it in the context of computer architectures, and in particular of other CGRAs. The book starts with an extensive evaluation of historic and existing CGRAs and their strengths and weaknesses. This also leads to a better understanding and new definition of what distinguishes CGRAs from other architectural approaches. The authors introduce Blocks as unique due to its separate programmable control and data paths, allowing light-weight instruction decode units to be arbitrarily connected to one or more functional units (FUs) over a statically configured interconnect. The discussion includes an explanation of how to model architectures, resulting in an area and energy model for Blocks. The accuracy of this model is evaluated against fully implemented architectures, showing that although it is

three orders of magnitude faster than synthesis the error margin is very acceptable. The book concludes with a case study on a real System-on-Chip, including a RISC architecture, the Blocks CGRA and peripherals. Provides a comprehensive overview of many coarse-grained reconfigurable architectures (CGRAs) proposed in the last 25 years, as well as a classification of those CGRAs; Offers a new view on the positioning of CGRAs; Provides an in-depth description of structure of the Blocks CGRA and its unique aspects; Includes an extensive evaluation of various performance aspects of Blocks, such as performance, energy and area, as well as a comparison with various traditional approaches; Uses a case study showing how Blocks can be used in a real system on-chip, and how performance of this system-on-chip can be estimated using the proposed model.