1. Record Nr. UNINA9910485047503321

Titolo	Reconfigurable Computing: Architectures, Tools, and Applications : 4th International Workshop, ARC 2008, London, UK, March 26-28, 2008, Proceedings / / edited by Roger Woods, Katherine Compton, Christos Bourganis, Pedro C. Diniz
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2008
ISBN	3-540-78610-4
Edizione	[1st ed. 2008.]
Descrizione fisica	1 online resource (XIV, 346 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 4943
Disciplina	004
Soggetti	Computer science Computers Microprocessors Computer architecture Computer networks Electronic digital computers—Evaluation Computer systems Theory of Computation Computer Hardware Processor Architectures Computer Communication Networks System Performance and Evaluation Computer System Implementation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Keynotes -- Synthesizing FPGA Circuits from Parallel Programs -- From Silicon to Science: The Long Road to Production Reconfigurable Supercomputing -- The von Neumann Syndrome and the CS Education Dilemma -- Programming and Compilation -- Optimal Unroll Factor for Reconfigurable Architectures -- Programming Reconfigurable Decoupled Application Control Accelerator for Mobile Systems -- DNA and String Processing Applications -- DNA Physical Mapping on a

Reconfigurable Platform -- Hardware BLAST Algorithms with Multi-seeds Detection and Parallel Extension -- Highly Space Efficient Counters for Perl Compatible Regular Expressions in FPGAs -- Scientific Applications -- A Custom Processor for a TDMA Solver in a CFD Application -- A High Throughput FPGA-Based Floating Point Conjugate Gradient Implementation -- Reconfigurable Computing Hardware and Systems -- Physical Design of FPGA Interconnect to Prevent Information Leakage -- Symmetric Multiprocessor Design for Hybrid CPU/FPGA SoCs -- Run-Time Adaptable Architectures for Heterogeneous Behavior Embedded Systems -- Image Processing -- FPGA-Based Real-Time Super-Resolution on an Adaptive Image Sensor -- A Parallel Hardware Architecture for Image Feature Detection -- Reconfigurable HW/SW Architecture of a Real-Time Driver Assistance System -- Run-Time Behavior -- A New Self-managing Hardware Design Approach for FPGA-Based Reconfigurable Systems -- A Preemption Algorithm for a Multitasking Environment on Dynamically Reconfigurable Processor -- Accelerating Speculative Execution in High-Level Synthesis with Cancel Tokens -- Instruction Set Extension -- ARISE Machines: Extending Processors with Hybrid Accelerators -- The Instruction-Set Extension Problem: A Survey -- Random Number Generation and Financial Computation -- An FPGA Run-Time Parameterisable Log-Normal Random Number Generator -- Multivariate Gaussian Random Number Generator Targeting Specific Resource Utilization in an FPGA -- Exploring Reconfigurable Architectures for Binomial-Tree Pricing Models -- Posters -- Hybrid-Mode Floating-Point FPGA CORDIC Co-processor -- Multiplier-Based Double Precision Floating Point Divider According to the IEEE-754 Standard -- Creating the World’s Largest Reconfigurable Supercomputing System Based on the Scalable SGI® Altix® 4700 System Infrastructure and Benchmarking Life-Science Applications -- Highly Efficient Structure of 64-Bit Exponential Function Implemented in FPGAs -- A Framework for the Automatic Generation of Instruction-Set Extensions for Reconfigurable Architectures -- PARO: Synthesis of Hardware Accelerators for Multi-dimensional Dataflow-Intensive Applications -- Stream Transfer Balancing Scheme Utilizing Multi-path Routing in Networks on Chip -- Efficiency of Dynamic Reconfigurable Datapath Extensions – A Case Study -- Online Hardware Task Scheduling and Placement Algorithm on Partially Reconfigurable Devices -- Data Reallocation by Exploiting FPGA Configuration Mechanisms -- A Networked, Lightweight and Partially Reconfigurable Platform -- Neuromolecularware – A Bio-inspired Evolvable Hardware and Its Application to Medical Diagnosis -- An FPGA Configuration Scheme for Bitstream Protection -- Lossless Compression for Space Imagery in a Dynamically Reconfigurable Architecture.