1. Record Nr. UNINA9910485011303321

Titolo	Applied Reconfigurable Computing : 11th International Symposium, ARC 2015, Bochum, Germany, April 13-17, 2015, Proceedings / / edited by Kentaro Sano, Dimitrios Soudris, Michael Hübner, Pedro C. Diniz
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2015
ISBN	3-319-16214-4
Edizione	[1st ed. 2015.]
Descrizione fisica	1 online resource (XVIII, 557 p. 257 illus.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 9040
Disciplina	004
Soggetti	Computers Computer engineering Computer networks Algorithms Artificial intelligence Application software Computer Hardware Computer Engineering and Networks Artificial Intelligence Computer and Information Systems Applications
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Architecture and Modeling -- Reducing Storage Costs of Reconfiguration Contexts by Sharing Instruction Memory Cache Blocks -- A Vector Caching Scheme for Streaming FPGA SpMV Accelerators -- Hierarchical Dynamic Power-Gating in FPGAs -- Tools and Compilers -- Hardware Synthesis from Functional Embedded Domain-Specific Languages: A Case Study in Regular Expression Compilation -- ArchHDL: A Novel Hardware RTL Design Environment in C++ -- Operand-Value-Based Modeling of Dynamic Energy Consumption of Soft Processors in FPGA -- Systems and Applications -- Preemptive Hardware Multitasking in ReconOS -- A Fully Parallel Particle Filter Architecture for FPGAs -- TEAChER: TEach AdvanCEd Reconfigurable

Architectures and Tools -- Tools and Compilers -- Dynamic Memory Management in Vivado-HLS for Scalable Many-Accelerator Architectures -- SET-PAR: Place and Route Tools for the Mitigation of Single Event Transients on Flash-Based FPGAs -- Advanced SystemC Tracing and Analysis Framework for Extra-Functional Properties -- Run-Time Partial Reconfiguration Simulation Framework Based on Dynamically Loadable Components -- Network-on-a-Chip Architecture Virtualization for Run-Time Hardware Multithreading on Field Programmable Gate Arrays -- Centralized and Software-Based Run-Time Traffic Management Inside Configurable Regions of Interest in Mesh-Based Networks-on-Chip -- Survey on Real-Time Network-on-Chip Architectures -- Cryptography Applications Efficient SR-Latch PUF -- Hardware Benchmarking of Cryptographic Algorithms Using High-Level Synthesis Tools: The SHA-3 Contest Case Study -- Dual CLEFIA/AES Cipher Core on FPGA -- Systems and Applications -- An Efficient and Flexible FPGA Implementation of a Face Detection System -- A Flexible Software Framework for Dynamic Task Allocation on MPSoCs Evaluated in an Automotive Context -- A Dynamically Reconfigurable Mixed Analog-Digital Filter Bank -- The Effects of System Hyper Pipelining on Three Computational Benchmarks Using FPGAs -- Extended Abstracts (Posters) -- A Timing Driven Cycle-Accurate Simulation for Coarse-Grained Reconfigurable Architectures -- Scalable and Efficient Linear Algebra Kernel Mapping for Low Energy Consumption on the Layers CGRA. -- A Novel Concept for Adaptive Signal Processing on Reconfigurable Hardware -- Evaluation of High-Level Synthesis Techniques for Memory and Datapath Tradeoffs in FPGA Based SoC Architectures -- Measuring Failure Probability of Coarse and Fine Grain TMR Schemes in SRAM-based FPGAs Under Neutron-Induced Effects -- Modular Acquisition and Stimulation System for Timestamp-Driven Neuroscience Experiments -- DRAM Row Activation Energy Optimization for Stride Memory Access on FPGA-Based Systems -- Acceleration of Data Streaming Classification Using Reconfigurable Technology -- On-The-Fly Verification of Reconfigurable Image Processing Modules Based on a Proof-Carrying Hardware Approach -- Partial Reconfiguration for Dynamic Mapping of Task Graphs onto 2D Mesh Platform -- A Challenge of Portable and High-Speed FPGA Accelerator -- Total Ionizing Dose Effects of Optical Components on an Optically Reconfigurable Gate Array -- Exploring Dynamic Reconfigurable CORDIC Co-Processors Tightly Coupled with a VLIW-SIMD Soft-Processor Architecture -- Mesh of Clusters FPGA Architectures: Exploration Methodology and Interconnect Optimization -- DyAFNoC: Dynamically Reconfigurable NoC Characterization Using a Simple Adaptive Deadlock-Free Routing Algorithm with a Low Implementation Cost -- A Flexible Multilayer Perceptron Co-processor for FPGAs -- Reconfigurable Hardware Assist for Linux Process Scheduling in Heterogeneous Multicore SoCs -- Towards Performance Modeling of 3D Memory Integrated FPGA Architectures -- Pyverilog: A Python-Based Hardware Design Processing Toolkit for Verilog HDL -- Special Session 1: Funded R&D Running and Completed Projects (Invited Papers) -- Towards Unification of Accelerated Computing and Interconnection For Extreme-Scale Computing -- SPARTAN/SEXTANT/COMPASS: Advancing Space Rover Vision via Reconfigurable Platforms -- Hardware Task Scheduling for Partially Reconfigurable FPGAs -- SWAN-iCARE Project: On the Efficiency of FPGAs Emulating Wearable Medical Devices for Wound Management and Monitoring -- Special Session 2: Horizon 2020 Funded Projects (Invited Papers) -- DynamIA: Dynamic Hardware Reconfiguration in Industrial Applications -- Robots in Assisted Living Environments as an

Unobtrusive, Efficient, Reliable and Modular Solution for Independent Ageing: The RADIO Perspective -- Reconfigurable Computing for Analytics Acceleration of Big Bio-Data: The AEGLE Approach -- COSSIM : A Novel, Comprehensible, Ultra-Fast, Security-Aware CPS Simulator.

Sommario/riassunto

This book constitutes the refereed proceedings of the 11th International Symposium on Applied Reconfigurable Computing, ARC 2015, held in Bochum, Germany, in April 2015. The 23 full papers and 20 short papers presented in this volume were carefully reviewed and selected from 85 submissions. They are organized in topical headings named: architecture and modeling; tools and compilers; systems and applications; network-on-a-chip; cryptography applications; extended abstracts of posters. In addition, the book contains invited papers on funded R&D - running and completed projects and Horizon 2020 funded projects.