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Titolo	Technology mapping for LUT-based FPGA // Marcin Kubica, Adam Opara, Dariusz Kania
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Edizione	[1st ed. 2021.]
Descrizione fisica	1 online resource (IX, 207 p. 111 illus., 53 illus. in color.)
Collana	Lecture notes in electrical engineering ; ; Volume 713
Disciplina	621.395
Soggetti	Field programmable gate arrays
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di contenuto	Introduction -- Methods for representing Boolean Functions - basic definitions -- Binary decision diagrams (BDD) -- Theoretical basis of decomposition -- Decomposition of functions described using BDD -- Ordering variables in BDD diagrams -- Nondisjoint decomposition -- Decomposition of multioutput functions described using BDD -- Partial sharing of logic resources -- Ability of the configuration of configurable logic blocks.
Sommario/riassunto	This book covers selected topics of automated logic synthesis dedicated to FPGAs. The authors focused on two main problems: decomposition of the multioutput functions and technology mapping. Additionally, the idea of using binary decision diagrams (BDD) in these processes was presented. The book is a scientific monograph summarizing the authors' many years of research. As a result, it contains a large number of experimental results, which makes it a valuable source for other researchers. The book has a significant didactic value. Its arrangement allows for a gradual transition from basic things (e.g., description of logic functions) to much more complex issues. This approach allows less advanced readers to better understand the described problems. In addition, the authors made sure that the issues described in the book were supported by practical examples, thanks to which the reader can independently analyze even the most complex problems described in the book.

