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Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	FSM-Based Models of Control Units -- Structural decomposition in FSM synthesis -- Twofold State Assignment for Mealy FSMs -- Twofold state assignment for Moore FSMs -- Combining twofold state assignment with transformation of object codes -- Combining twofold state assignment with replacement of logical conditions -- Mixed encoding of microoperations -- Synthesis of Mealy FSMs with counters.
Sommario/riassunto	This book focuses on control units, which are a vital part of modern digital systems, and responsible for the efficiency of controlled systems. The model of a finite state machine (FSM) is often used to represent the behavior of a control unit. As a rule, control units have irregular structures that make it impossible to design their logic circuits using the standard library cells. Design methods depend strongly on such factors as the FSM used, specific features of the logic elements implemented in the FSM logic circuit, and the characteristics of the control algorithm to be interpreted. This book discusses Moore and Mealy FSMs implemented with FPGA chips, including look-up table elements (LUT) and embedded memory blocks (EMB). It is crucial to minimize the number of LUTs and EMBs in an FSM logic circuit, as well as to make the interconnections between the logic elements more regular, and various methods of structural decompositions can be used to solve this problem. These methods are reduced to the presentation

of an FSM circuit as a composition of different logic blocks, the majority of which implement systems of intermediate logic functions different (and much simpler) than input memory functions and FSM output functions. The structural decomposition results in multilevel FSM circuits having fewer logic elements than equivalent single-level circuits. The book describes well-known methods of structural decomposition and proposes new ones, examining their impact on the final amount of hardware in an FSM circuit. It is of interest to students and postgraduates in the area of Computer Science, as well as experts involved in designing digital systems with complex control units. The proposed models and design methods open new possibilities for creating logic circuits of control units with an optimal amount of hardware and regular interconnections. .
