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Record Nr.	UNINA9910484761203321
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Titolo	Design for testability, debug and reliability : next generation measures using formal techniques / / Sebastian Huhn, Rolf Drechsler
Pubbl/distr/stampa	Cham, Switzerland : , : Springer, , [2021] ©2021
ISBN	3-030-69209-4
Descrizione fisica	1 online resource (177 pages)
Disciplina	621.3815
Soggetti	Integrated circuits - Design and construction Integrated circuits - Reliability Integrated circuits - Testing Debugging in computer science
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Sommario/riassunto	This book introduces several novel approaches to pave the way for the next generation of integrated circuits, which can be successfully and reliably integrated, even in safety-critical applications. The authors describe new measures to address the rising challenges in the field of design for testability, debug, and reliability, as strictly required for state-of-the-art circuit designs. In particular, this book combines formal techniques, such as the Satisfiability (SAT) problem and the Bounded Model Checking (BMC), to address the arising challenges concerning the increase in test data volume, as well as test application time and the required reliability. All methods are discussed in detail and evaluated extensively, while considering industry-relevant benchmark candidates. All measures have been integrated into a common framework, which implements standardized software/hardware interfaces. Provides readers with a combination of a comprehensive set of formal techniques covering and enhancing different aspects of the state-of-the-art design and test flow for ICs; Introduces newly developed heuristic, formal optimization-based and partition-based retargeting techniques and integrates them into a

common framework; Describes fully compliant (with respect to industrial de-facto standard) measures to enhance the DFT, DFD and DFR capabilities while supporting standardized data exchange formats; Includes new measures to tackle shortcomings of existing state-of-the-art methods, including zero-defect enforcing safety-critical applications.