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Nota di contenuto	Session 1 - High-Level Design (1) -- System-Level Application-Specific NoC Design for Network and Multimedia Applications -- Fast and Accurate Embedded Systems Energy Characterization Using Non-intrusive Measurements -- A Flexible General-Purpose Parallelizing Architecture for Nested Loops in Reconfigurable Platforms -- An Automatic Design Flow for Mapping Application onto a 2D Mesh NoC

Architecture -- Session 2 - Low Power Design Techniques -- Template Vertical Dictionary-Based Program Compression Scheme on the TTA -- Asynchronous Functional Coupling for Low Power Sensor Network Processors -- A Heuristic for Reducing Dynamic Power Dissipation in Clocked Sequential Designs -- Low-Power Content Addressable Memory With Read/Write and Matched Mask Ports -- The Design and Implementation of a Power Efficient Embedded SRAM -- Session 3 - Low Power Analog Circuits -- Design of a Linear Power Amplifier with ±1.5V Power Supply Using ALADIN -- Settling Time Minimization of Operational Amplifiers -- Low-Voltage Low-Power Curvature-Corrected Voltage Reference Circuit Using DTMOSTs -- Session 4 - Statistical Static Timing Analysis -- Computation of Joint Timing Yield of Sequential Networks Considering Process Variations -- A Simple Statistical Timing Analysis Flow and Its Application to Timing Margin Evaluation -- A Statistical Approach to the Timing-Yield Optimization of Pipeline Circuits -- Session 5 - Power Modeling and Optimization -- A Novel Gate-Level NBTI Delay Degradation Model with Stacking Effect -- Modelling the Impact of High Level Leakage Optimization Techniques on the Delay of RT-Components -- Logic Style Comparison for Ultra Low Power Operation in 65nm Technology -- Design-In Reliability for 90-65nm CMOS Nodes Submitted to Hot-Carriers and NBTI Degradation -- Session 6 - Low Power RoutingOptimization -- Clock Distribution Techniques for Low-EMI Design -- Crosstalk Waveform Modeling Using Wave Fitting -- Weakness Identification for Effective Repair of Power Distribution Network -- New Adaptive Encoding Schemes for Switching Activity Balancing in On-Chip Buses -- On the Necessity of Combining Coding with Spacing and Shielding for Improving Performance and Power in Very Deep Sub-micron Interconnects -- Session 7 - High Level Design (2) -- Soft Error-Aware Power Optimization Using Gate Sizing -- Automated Instruction Set Characterization and Power Profile Driven Software Optimization for Mobile Devices -- RTL Power Modeling and Estimation of Sleep Transistor Based Power Gating -- Functional Verification of Low Power Designs at RTL -- XEEMU: An Improved XScale Power Simulator -- Session 8 - Security and Asynchronous Design -- Low Power Elliptic Curve Cryptography -- Design and Test of Self-checking Asynchronous Control Circuit -- An Automatic Design Flow for Implementation of Side Channel Attacks Resistant Crypto-Chips -- Analysis and Improvement of Dual Rail Logic as a Countermeasure Against DPA -- Session 9 - Low Power Applications -- Performance Optimization of Embedded Applications in a Hybrid Reconfigurable Platform -- The Energy Scalability of Wavelet-Based, Scalable Video Decoding -- Direct Memory Access Optimization in Wireless Terminals for Reduced Memory Latency and Energy Consumption -- Poster 1 - Modeling and Optimization -- Exploiting Input Variations for Energy Reduction -- A Model of DPA Syndrome and Its Application to the Identification of Leaking Gates -- Static Power Consumption in CMOS Gates Using Independent Bodies -- Moderate Inversion: Highlights for Low Voltage Design -- On Two-Pronged Power-Aware Voltage Scheduling for Multi-processor Real-Time Systems -- SemiCustom Design: A Case Study on SIMD Shufflers -- Poster 2 - High Level Design -- Optimization for Real-Time Systems with Non-convex Power Versus Speed Models -- Triple-Threshold Static Power Minimization in High-Level Synthesis of VLSI CMOS -- A Fast and Accurate Power Estimation Methodology for QDI Asynchronous Circuits -- Subthreshold Leakage Modeling and Estimation of General CMOS Complex Gates -- A Platform for Mixed HW/SW Algorithm Specifications for the Exploration of SW and HW Partitioning -- Fast Calculation of Permissible Slowdown Factors for Hard Real-Time

Systems -- Design Methodology and Software Tool for Estimation of Multi-level Instruction Cache Memory Miss Rate -- Poster 3 - Low Power Techniques and Applications -- A Statistical Model of Logic Gates for Monte Carlo Simulation Including On-Chip Variations -- Switching Activity Reduction of MAC-Based FIR Filters with Correlated Input Data -- Performance of CMOS and Floating-Gate Full-Adders Circuits at Subthreshold Power Supply -- Low-Power Digital Filtering Based on the Logarithmic Number System -- A Power Supply Selector for Energy- and Area-Efficient Local Dynamic Voltage Scaling -- Dependability Evaluation of Time-Redundancy Techniques in Integer Multipliers -- Keynotes -- Design and Industrialization Challenges of Memory Dominated SOCs -- Statistical Static Timing Analysis: A New Approach to Deal with Increased Process Variability in Advanced Nanometer Technologies -- Analog Power Modelling -- Industrial Session - Design Challenges in Real-Life Projects -- Technological Trends, Design Constraints and Design Implementation Challenges in Mobile Phone Platforms -- System Design from Instrument Level Down to ASIC Transistors with Speed and Low Power as Driving Parameters.

Sommario/riassunto

th Welcome to the proceedings of PATMOS 2007, the 17 in a series of international workshops. PATMOS 2007 was organized by Chalmers University of Technology with IEEE Sweden Chapter of the Solid-State Circuit Society technical - sponsorship and IEEE CEDA sponsorship. Over the years, PATMOS has evolved into an important European event, where - searchers from both industry and academia discuss and investigate the emerging ch- lenges in future and contemporary applications, design methodologies, and tools - quired for the development of the upcoming generations of integrated circuits and systems. The technical program of PATMOS 2007 consisted of state-of-the-art te- nical contributions, three invited talks and an industrial session on design challenges in real-life projects. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on m- eling, design, characterization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert - viewers, selected the 55 papers presented at PATMOS. The papers were organized into 9 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, full papers were required, and several reviews were received per manuscript.