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Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 5798
Classificazione	DAT 516f SS 4800
Altri autori (Persone)	FrachtenbergEitan SchwiegelshohnUwe <1958->
Disciplina	004n/a
Soggetti	Operating systems (Computers) Software engineering Microprocessors Computer architecture Computers Logic design Operating Systems Software Engineering Processor Architectures Hardware Performance and Reliability Logic Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di contenuto	Dynamic Resource-Critical Workflow Scheduling in Heterogeneous Environments -- Decentralized Grid Scheduling with Evolutionary Fuzzy Systems -- Analyzing the EGEE Production Grid Workload: Application to Jobs Submission Optimization -- The Resource Usage Aware Backfilling -- The Gain of Overbooking -- Modeling Parallel System Workloads with Temporal Locality -- Scheduling Restartable Jobs with Short Test Runs -- Effects of Topology-Aware Allocation Policies on Scheduling Performance -- Contention-Aware Scheduling with Task

Duplication -- Job Admission and Resource Allocation in Distributed Streaming Systems -- Scalability Analysis of Job Scheduling Using Virtual Nodes -- Competitive Two-Level Adaptive Scheduling Using Resource Augmentation -- Job Scheduling with Lookahead Group Matchmaking for Time/Space Sharing on Multi-core Parallel Machines -- Adaptive Scheduling for QoS Virtual Machines under Different Resource Allocation – Performance Effects and Predictability -- Limits of Work-Stealing Scheduling.

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Sommario/riassunto

This book constitutes the revised papers of the 14th International Workshop on Job Scheduling Strategies for Parallel Processing, JSSPP 2009, which was held in Rome, Italy, in May 2009. The 15 revised papers presented were carefully reviewed and selected from 25 submissions. The papers cover all current issues of job scheduling strategies for parallel processing; this year the conference had an increasing trend towards heterogeneous and multi-core architectures.

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