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Nota di contenuto	Keynote Address I -- Processor Architecture for Trustworthy Computers -- Session 1A: Energy Efficient and Power Aware Techniques -- Efficient Voltage Scheduling and Energy-Aware Co-synthesis for Real-Time Embedded Systems -- Energy-Effective

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Sommario/riassunto

On behalf of the ProgramCommittee, we are pleased to present the proceedings of the 2005 Asia-Paci?c Computer Systems Architecture Conference (ACSAC 2005) held in the beautiful and dynamic country of Singapore. This conference was the tenth in its series, one of the leading forums for sharing the emerging research ?ndings in this ?eld. In consultation with the ACSAC Steering Committee, we selected a - member Program Committee. This Program Committee represented a broad spectrum of research expertise to ensure a good balance of research areas, - stitutions and experience while maintaining the high quality of this conference series. This year’s committee was of the same size as last year but had 19 new faces. We received a total of 173 submissions which is 14% more than last year. Each paper was assigned to at least three and in some cases four ProgramC- mittee members for review. Wherever necessary, the committee members called upon the expertise of their colleagues to ensure the highest possible quality in the reviewing process. As a result, we received 415 reviews from the Program Committee members and their 105 co-reviewers whose names are acknowledged inthe proceedings.Theconferencecommitteeadopteda systematicblind review process to provide a fair assessment of all submissions. In the end, we accepted 65 papers on a broad range of topics giving an acceptance rate of 37.5%. We are grateful to all the Program Committee members and the co-reviewers for their e?orts in completing the reviews within a tight schedule.