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Nota di contenuto	Beachnote -- What Else Is Broken? Can We Fix It? -- Architectures for Multimedia -- Programmable and Scalable Architecture for Graphics Processing Units -- The Abstract Streaming Machine: Compile-Time Performance Modelling of Stream Programs on Heterogeneous Multiprocessors -- CABAC Accelerator Architectures for Video Compression in Future Multimedia: A Survey -- Programmable Accelerators for Reconfigurable Video Decoder -- Scenario Based

Mapping of Dynamic Applications on MPSoC: A 3D Graphics Case Study -- Multiple Description Scalable Coding for Video Transmission over Unreliable Networks -- Multi/Many Cores Architectures -- Evaluation of Different Multithreaded and Multicore Processor Configurations for SoPC -- Implementing Fine/Medium Grained TLP Support in a Many-Core Architecture -- Implementation of W-CDMA Cell Search on a FPGA Based Multi-Processor System-on-Chip with Power Management -- A Multiprocessor Architecture with an Omega Network for the Massively Parallel Model GCA -- VLSI Architectures Design -- Towards Automated FSMD Partitioning for Low Power Using Simulated Annealing -- Radix-4 Recoded Multiplier on Quantum-Dot Cellular Automata -- Prediction in Dynamic SDRAM Controller Policies -- Inversion/Non-inversion Implementation for an 11,424 Gate-Count Dynamic Optically Reconfigurable Gate Array VLSI -- Architecture Modeling and Exploration Tools -- Visualization of Computer Architecture Simulation Data for System-Level Design Space Exploration -- Modeling Scalable SIMD DSPs in LISA -- NoGAP: A Micro Architecture Construction Framework -- A Comparison of NoTA and GENESYS -- Special Session 1: Instruction-Set Customization -- to Instruction-Set Customization -- Constraint-Driven Identification of Application Specific Instructions in the DURASE System -- A Generic Design Flow for Application Specific Processor Customization through Instruction-Set Extensions (ISEs) -- Runtime Adaptive Extensible Embedded Processors — A Survey -- Special Session 2: The Future of Reconfigurable Computing and Processor Architectures -- to the Future of Reconfigurable Computing and Processor Architectures -- An Embrace-and-Extend Approach to Managing the Complexity of Future Heterogeneous Systems -- Applying the Stream-Based Computing Model to Design Hardware Accelerators: A Case Study -- Reconfigurable Multicore Server Processors for Low Power Operation -- Reconfigurable Computing in the New Age of Parallelism -- Reconfigurable Multithreading Architectures: A Survey -- Special Session 3: Mastering Cell BE and GPU Execution Platforms -- to Mastering Cell BE and GPU Execution Platforms -- Efficient Mapping of Multiresolution Image Filtering Algorithms on Graphics Processors -- Implementing Blocked Sparse Matrix-Vector Multiplication on NVIDIA GPUs -- Experiences with Cell-BE and GPU for Tomography -- Realizing FIFO Communication When Mapping Kahn Process Networks onto the Cell -- Exploiting Locality on the Cell/B.E. through Bypassing -- Exploiting the Cell/BE Architecture with the StarPU Unified Runtime System.

Sommario/riassunto

This book constitutes the refereed proceedings of the 9th International Workshop on Architectures, Modeling, and Simulation, SAMOS 2009, held on Samos, Greece, on July 20-23, 2009. The 18 regular papers presented were carefully reviewed and selected from 52 submissions. The papers are organized in topical sections on architectures for multimedia, multi/many cores architectures, VLSI architectures design, architecture modeling and exploration tools. In addition there are 14 papers from three special sessions which were organized on topics of current interest: instruction-set customization, reconfigurable computing and processor architectures, and mastering cell BE and GPU execution platforms.