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Nota di contenuto	Keynotes -- FPGA Design Productivity – A Discussion of the State of the Art and a Research Agenda -- Resiliency in Elemental Computing -- The Colour of Embedded Computation -- Applications 1 -- A HyperTransport 3 Physical Layer Interface for FPGAs -- Parametric Design for Reconfigurable Software-Defined Radio -- Applications 2 -- Hardware/Software FPGA Architecture for Robotics Applications -- Reconfigurable Operator Based Multimedia Embedded Processor --

FPGA Security and Bitstream Analysis -- A Protocol for Secure Remote Updates of FPGA Configurations -- FPGA Analysis Tool: High-Level Flows for Low-Level Design Analysis in Reconfigurable Computing -- Fault Tolerant Systems -- An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications -- Timing Driven Placement for Fault Tolerant Circuits Implemented on SRAM-Based FPGAs -- Architectures -- A Novel Local Interconnect Architecture for Variable Grain Logic Cell -- Dynamically Adapted Low Power ASIPs -- Fast Optical Reconfiguration of a Nine-Context DORGA -- Place and Route Techniques -- Heterogeneous Architecture Exploration: Analysis vs. Parameter Sweep -- On Simplifying Placement and Routing by Extending Coarse-Grained Reconfigurable Arrays with Omega Networks -- A New Datapath Merging Method for Reconfigurable System -- Cryptography -- Optimizing the Control Hierarchy of an ECC Coprocessor Design on an FPGA Based SoC Platform -- Fully Pipelined Hardware Implementation of 128-Bit SEED Block Cipher Algorithm -- Improving Throughput of AES-GCM with Pipelined Karatsuba Multipliers on FPGAs -- Resource Allocation and Scheduling -- Compiling Techniques for Coarse Grained Runtime Reconfigurable Architectures -- Online Task Scheduling for the FPGA-Based Partially Reconfigurable Systems -- Applications 3 -- Word-Length Optimization and Error Analysis of a Multivariate Gaussian Random Number Generator -- FPGA-Based Anomalous Trajectory Detection Using SOFM -- Posters -- SORU: A Reconfigurable Vector Unit for Adaptable Embedded Systems -- A Parallel Branching Program Machine for Emulation of Sequential Circuits -- Memory Sharing Approach for TMR Softcore Processor -- The Need for Reconfigurable Routers in Networks-on-Chip -- Transparent Dynamic Reconfiguration as a Service of a System-Level Middleware -- Optimizing Memory Access Latencies on a Reconfigurable Multimedia Accelerator: A Case of a Turbo Product Codes Decoder -- Tile-Based Fault Tolerant Approach Using Partial Reconfiguration -- Regular Expression Pattern Matching Supporting Constrained Repetitions -- Accelerating Calculations on the RASC Platform: A Case Study of the Exponential Function -- AES-Galois Counter Mode Encryption/Decryption FPGA Core for Industrial and Residential Gigabit Ethernet Communications -- CCproc: A Custom VLIW Cryptography Co-processor for Symmetric-Key Ciphers -- Object Tracking and Motion Capturing in Hardware-Accelerated Multi-camera System -- Implementation of the AES Algorithm for a Reconfigurable, Bit Serial, Fully Pipelined Architecture -- A Hardware Accelerated Simulation Environment for Spiking Neural Networks -- Survey of Advanced CABAC Accelerator Architectures for Future Multimedia -- Real Time Simulation in Floating Point Precision Using FPGA Computing -- A Hardware Analysis of Twisted Edwards Curves for an Elliptic Curve Cryptosystem -- A Seamless Virtualization Approach for Transparent Dynamical Function Mapping Targeting Heterogeneous and Reconfigurable Systems -- Pipeline Scheduling with Input Port Constraints for an FPGA-Based Biochemical Simulator -- ACCFS – Operating System Integration of Computational Accelerators Using a VFS Approach -- A Multithreaded Framework for Sequential Monte Carlo Methods on CPU/FPGA Platforms.

Sommario/riassunto

This book constitutes the refereed proceedings of the 5th International Workshop on Applied Reconfigurable Computing, ARC 2009, held in Karlsruhe, Germany, in March 2009. The 21 full papers and 21 short papers presented together with the abstracts of 3 keynote lectures were carefully reviewed and selected from about 100 submissions. The papers are organized in topical sections on FPGA security and bitstream

analysis, fault tolerant systems, architectures, place and route techniques, cryptography, and resource allocation and scheduling, as well as on applications.