

1. Record Nr.	UNINA9910484352003321
Titolo	Computer Aided Verification : 19th International Conference, CAV 2007, Berlin, Germany, July 3-7, 2007, Proceedings // edited by Werner Damm, Holger Hermanns
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2007
ISBN	3-540-73368-X
Edizione	[1st ed. 2007.]
Descrizione fisica	1 online resource (XV, 562 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 4590
Disciplina	006.3
Soggetti	Computer science Software engineering Machine theory Artificial intelligence Logic design Theory of Computation Computer Science Logic and Foundations of Programming Software Engineering Formal Languages and Automata Theory Artificial Intelligence Logic Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Invited Talks -- Automatically Proving Program Termination -- A Mathematical Approach to RTL Verification -- Software Bugs Seen from an Industrial Perspective or Can Formal Methods Help on Automotive Software Development? -- Invited Tutorials -- Algorithms for Interface Synthesis -- A Tutorial on Satisfiability Modulo Theories -- A JML Tutorial: Modular Specification and Verification of Functional Behavior for Java -- Verification of Hybrid Systems -- Session I: Compositionality -- SAT-Based Compositional Verification Using Lazy Learning -- Local Proofs for Global Safety Properties -- Session II: Verification Process -- Low-Level Library Analysis and Summarization -- Verification Across Intellectual Property Boundaries -- Session III: Timed Synthesis and

Games -- On Synthesizing Controllers from Bounded-Response Properties -- An Accelerated Algorithm for 3-Color Parity Games with an Application to Timed Games -- UPPAAL-Tiga: Time for Playing Games! -- The TASM Toolset: Specification, Simulation, and Formal Verification of Real-Time Systems -- Session IV: Infinite State Verification -- Systematic Acceleration in Regular Model Checking -- Parameterized Verification of Infinite-State Processes with Global Conditions -- Session V: Tool Environment -- CADP 2006: A Toolbox for the Construction and Analysis of Distributed Processes -- jMoped: A Test Environment for Java Programs -- Hector: Software Model Checking with Cooperating Analysis Plugins -- The Why/Krakatoa/Caduceus Platform for Deductive Program Verification -- Session VI: Shapes -- Shape Analysis for Composite Data Structures -- Array Abstractions from Proofs -- Context-Bounded Analysis of Multithreaded Programs with Dynamic Linked Structures -- Revamping TVLA: Making Parametric Shape Analysis Competitive -- Session VII: Concurrent Program Verification -- Fast and Accurate Static Data-Race Detection for Concurrent Programs -- Parametric and Sliced Causality -- Spade: Verification of Multithreaded Dynamic and Recursive Programs -- Session VIII: Reactive Designs -- Anzu: A Tool for Property Synthesis -- RAT: A Tool for the Formal Analysis of Requirements -- Session IX: Parallelisation -- Parallelising Symbolic State-Space Generators -- I/O Efficient Accepting Cycle Detection -- Session X: Constraints and Decisions -- C32SAT: Checking C Expressions -- CVC3 -- BAT: The Bit-Level Analysis Tool -- LIRA: Handling Constraints of Linear Arithmetics over the Integers and the Reals -- Session XI: Probabilistic Verification -- Three-Valued Abstraction for Continuous-Time Markov Chains -- Magnifying-Lens Abstraction for Markov Decision Processes -- Underapproximation for Model-Checking Based on Random Cryptographic Constructions -- Session XII: Abstraction -- Using Counterexamples for Improving the Precision of Reachability Computation with Polyhedra -- Structural Abstraction of Software Verification Conditions -- An Abstract Domain for Analyzing Heap-Manipulating Low-Level Software -- Adaptive Symmetry Reduction -- Session XIII: Assume-Guarantee Reasoning -- From Liveness to Promptness -- Automated Assumption Generation for Compositional Verification -- Session XIV: Hybrid Systems -- Abstraction and Counterexample-Guided Construction of ϵ -Automata for Model Checking of Step-Discrete Linear Hybrid Models -- Test Coverage for Continuous and Hybrid Systems -- Hybrid Systems: From Verification to Falsification -- Session XV: Program Analysis -- Comparison Under Abstraction for Verifying Linearizability -- Leaping Loops in the Presence of Abstraction -- Configurable Software Verification: Concretizing the Convergence of Model Checking and Program Analysis -- Session XVI: SAT and Decision Procedures -- A Decision Procedure for Bit-Vectors and Arrays -- Boolean Abstraction for Temporal Logic Satisfiability -- A Lazy and Layered SMT() Solver for Hard Industrial Verification Problems.

Sommario/riassunto

This volume contains the proceedings of the International Conference on Computer Aided Verification (CAV), held in Berlin, Germany, July 3–7, 2007. CAV 2007 was the 19th in a series of conferences dedicated to the advancement of the theory and practice of computer-assisted formal analysis methods for software and hardware systems. The conference covers the spectrum from theoretical results to concrete applications, with an emphasis on practical verification tools and the algorithms and techniques that are needed for their implementation. We received 134 regular paper submissions and 39 tool paper submissions. Of these, the Program Committee selected 33

regular papers and 14 tool papers. Each submission was reviewed by at least three members of the Program Committee. The reviewing process included a PC review meeting, and – for the first time in the history of CAV – an author feedback period. About 50 additional reviews were provided by experts external to the Program Committee to assure a high quality selection. The CAV 2007 program included three invited talks from industry: – Byron Cook (Microsoft Research) on Automatically Proving Program Termination, – David Russinoff (AMD) on A Mathematical Approach to RTL Verification, and – Thomas Kropf (Bosch) on Software Bugs Seen from an Industrial Perspective.
