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Sommario/riassunto	This book evaluates the influence of process variations (e.g. work-function fluctuations) and radiation-induced soft errors in a set of logic cells using FinFET technology, considering the 7nm technological node as a case study. Moreover, for accurate soft error estimation, the authors adopt a radiation event generator tool (MUSCA SEP3), which deals both with layout features and electrical properties of devices. The authors also explore four circuit-level techniques (e.g. transistor reordering, decoupling cells, Schmitt Trigger, and sleep transistor) as alternatives to attenuate the unwanted effects on FinFET logic cells. This book also evaluates the mitigation tendency when different levels of process variation, transistor sizing, and radiation particle characteristics are applied in the design. An overall comparison of all methods addressed by this work is provided allowing to trace a trade-off between the reliability gains and the design penalties of each approach regarding the area, performance, power consumption, single

event transient (SET) pulse width, and SET cross-section. Explains how to measure the influence of process variability (e.g. work-function fluctuations) and radiation-induced soft errors in FinFET logic cells; Enables designers to improve the robustness of FinFET integrated circuits without focusing on manufacturing adjustments; Discusses the benefits and downsides of using circuit-level approaches such as transistor reordering, decoupling cells, Schmitt Trigger, and sleep transistor for mitigating the impact of process variability and soft errors; Evaluates the techniques described in the context of different test scenarios: distinct levels of process variations, transistor sizing, and different radiation features; Helps readers identify the best circuit design considering the target application and design requirements like area constraints or power/delay limitations.