

1. Record Nr.	UNINA9910484166103321
Titolo	Power-Aware Computer Systems : 4th International Workshop, PACS 2004, Portland, OR, USA, December 5, 2004, Revised Selected Papers / / edited by Babak Falsafi, T.N. Vijaykumar
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2005
ISBN	3-540-31485-7
Edizione	[1st ed. 2005.]
Descrizione fisica	1 online resource (X, 181 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 3471
Altri autori (Persone)	FalsafiBabak VijaykumarT. N. <1967->
Disciplina	621.3916
Soggetti	Computer engineering Computer networks Electronics Computer systems Computers Operating systems (Computers) Electrical engineering Computer Engineering and Networks Electronics and Microelectronics, Instrumentation Computer System Implementation Computer Hardware Operating Systems Electrical and Electronic Engineering
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Microarchitecture- and Circuit-Level Techniques -- An Optimized Front-End Physical Register File with Banking and Writeback Filtering -- Reducing Delay and Power Consumption of the Wakeup Logic Through Instruction Packing and Tag Memoization -- Bit-Sliced Datapath for Energy-Efficient High Performance Microprocessors -- Low-Overhead Core Swapping for Thermal Management -- Power-Aware Memory and Interconnect Systems -- Software–Hardware Cooperative Power

Management for Main Memory -- Energy-Aware Data Prefetching for General-Purpose Programs -- Bus Power Estimation and Power-Efficient Bus Arbitration for System-on-a-Chip Embedded Systems -- Context-Independent Codes for Off-Chip Interconnects -- Frequency-/Voltage-Scaling Techniques -- Dynamic Processor Throttling for Power Efficient Computations -- Effective Dynamic Voltage Scaling Through CPU-Boundedness Detection -- Safe Overprovisioning: Using Power Limits to Increase Aggregate Throughput -- Power Consumption Breakdown on a Modern Laptop -- Erratum -- Erratum.

Sommario/riassunto

Welcome to the proceedings of the Power-Aware Computer Systems (PACS 2004) workshop held in conjunction with the 37th Annual International Symposium on Microarchitecture (MICRO-37). The continued increase of power and energy dissipation in computer systems has resulted in higher cost, lower reliability, and reduced battery life in portable systems. Consequently, power and energy have become first-class constraints at all layers of modern computer systems. PACS 2004 is the fourth workshop in its series to explore techniques to reduce power and energy at all levels of computer systems and brings together academic and industry researchers. The papers in these proceedings span a wide spectrum of areas in power-aware systems. We have grouped the papers into the following categories: (1) microarchitecture- and circuit-level techniques, (2) power-aware memory and interconnect systems, and (3) frequency- and voltage-scaling techniques. The first paper in the microarchitecture group proposes banking and write-back filtering to reduce register file power. The second paper in this group optimizes both delay and power of the issue queue by packing two instructions in each issue queue entry and by memorizing upper-order bits of the wake-up tag. The third paper proposes bit slicing the datapath to exploit narrow width operations, and the last paper proposes to migrate application threads from one core to another in a multi-core chip to address thermal problems.
