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Soggetti	Compilers (Computer programs) Computer programming Computer science Computer networks Computer arithmetic and logic units Artificial intelligence - Data processing Compilers and Interpreters Programming Techniques Theory of Computation Computer Communication Networks Arithmetic and Logic Structures Data Science
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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Revisiting Graph Coloring Register Allocation: A Study of the Chaitin-Briggs and Callahan-Koblenz Algorithms -- Register Pressure in Software-Pipelined Loop Nests: Fast Computation and Impact on Architecture Design -- Manipulating MAXLIVE for Spill-Free Register Allocation -- Optimizing Packet Accesses for a Domain Specific Language on Network Processors -- Array Replication to Increase

Parallelism in Applications Mapped to Configurable Architectures -- Generation of Control and Data Flow Graphs from Scheduled and Pipelined Assembly Code -- Applying Data Copy to Improve Memory Performance of General Array Computations -- A Cache-Conscious Profitability Model for Empirical Tuning of Loop Fusion -- Optimizing Matrix Multiplication with a Classifier Learning System -- A Language for the Compact Representation of Multiple Program Versions -- Efficient Computation of May-Happen-in-Parallel Information for Concurrent Java Programs -- Evaluating the Impact of Thread Escape Analysis on a Memory Consistency Model-Aware Compiler -- Concurrency Analysis for Parallel Programs with Textually Aligned Barriers -- Titanium Performance and Potential: An NPB Experimental Study -- Efficient Search-Space Pruning for Integrated Fusion and Tiling Transformations -- Automatic Measurement of Instruction Cache Capacity -- Combined ILP and Register Tiling: Analytical Model and Optimization Framework -- Analytic Models and Empirical Search: A Hybrid Approach to Code Optimization -- Testing Speculative Work in a Lazy/Eager Parallel Functional Language -- Loop Selection for Thread-Level Speculation -- Software Thread Level Speculation for the Java Language and Virtual Machine Environment -- Lightweight Monitoring of the Progress of Remotely Executing Computations -- Using Platform-Specific Performance Counters for Dynamic Compilation -- A Domain-Specific Interpreter for Parallelizing a Large Mixed-Language Visualisation Application -- Compiler Control Power Saving Scheme for Multi Core Processors -- Code Transformations for One-Pass Analysis -- Scalable Array SSA and Array Data Flow Analysis -- Interprocedural Symbolic Range Propagation for Optimizing Compilers -- Parallelization of Utility Programs Based on Behavior Phase Analysis -- A Systematic Approach to Model-Guided Empirical Search for Memory Hierarchy Optimization -- An Efficient Approach for Self-scheduling Parallel Loops on Multiprogrammed Parallel Computers -- Dynamic Compilation for Reducing Energy Consumption of I/O-Intensive Applications -- Supporting SELL for High-Performance Computing -- Compiler Supports and Optimizations for PAC VLIW DSP Processors.

Sommario/riassunto

The 18th International Workshop on Languages and Compilers for High- Performance Computing was scheduled to be held in New Orleans, Louisiana, in October 2005.Unfortunately, because of the devastation caused by Hurricane Katrina the meeting needed to be moved. It was held in Hawthorne, New York, thanks to help from IBM. The workshopis an annual forum for leading research groups to present their current research activities and the latest results, cov- ing languages, compiler techniques, runtime environments, and compiler-related performance evaluation for parallel and high-performance computing. Sixty-?ve researchersfromCanada,France,Japan,Korea,P.R. China, Spain,Switzerland, Taiwan, UK, and the USA attended the workshop. Thirty-four research papers (26 regular papers and eight short papers) were presented at the workshop. These papers were reviewed by the Program C- mittee; external reviewers were used as needed. The authors then received - ditional comments during the workshop. The revisions after the workshop are now assembled into these ?nal proceedings. Wethank Siddhartha ChatterjeefromtheIBMT.J. WatsonResearchCenter for his keynote talk titled "The Changing Landscape of Parallel Computing." The workshop included a special session titled "High-Productivity Languages for HPC: Compiler Challenges" consisting of invited talks on the three l- guages being developed by the DARPA High-Productivity Computing Systems (HPCS) vendors.ThetalksweregivenbySteveDietz(fromCrayonthelanguage Chapel), Vivek Sarkar(from IBMon the languageX10), andDavid Chase

(from Sun on the languageFortress). Frederica Darema gavea presentation during the workshop banquet about the proposed Dynamic Data-Driven Applications S- tems (DDDAS) program at the US National Science Foundation.