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| Autore | Ghavami Behnam |
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| Soggetti | Integrated circuits - Very large scale integration - Reliability<br>Electronic circuits |
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| Nota di contenuto | Introduction: Soft Error Modeling -- Soft Error Rate Estimation of VLSI circuits -- Process Variation Aware Soft Error Rate Estimation Method for Integrated Circuits -- GPU-Accelerated Soft Error Rate Analysis of Large-scale Integrated Circuits -- FPGA Hardware Acceleration of Soft Error Rate Estimation of Digital Circuits -- Soft Error Tolerant Circuit Design using Partitioning-based Gate Sizing -- Resynthesize Technique for Soft Error Tolerant Design of Combinational Circuits. |
| Sommario/riassunto | This book is intended for readers who are interested in the design of robust and reliable electronic digital systems. The authors cover emerging trends in design of today’s reliable electronic systems which are applicable to safety-critical applications, such as automotive or healthcare electronic systems. The emphasis is on modeling approaches and algorithms for analysis and mitigation of soft errors in nano-scale CMOS digital circuits, using techniques that are the cornerstone of Computer Aided Design (CAD) of reliable VLSI circuits. The authors introduce software tools for analysis and mitigation of soft errors in electronic systems, which can be integrated easily with design flows. In addition to discussing soft error aware analysis techniques for combinational logic, the authors also describe new soft error mitigation strategies targeting commercial digital circuits. Coverage includes novel Soft Error Rate (SER) analysis techniques such as process variation aware SER estimation and GPU accelerated SER analysis techniques, in |

addition to SER reduction methods such as gate sizing and logic restructuring based SER techniques. Provides an accessible, comprehensive introduction to soft errors; Describes an easy to follow procedure for modeling, analysis, and estimation of soft error rate of digital circuits; Includes state-of-the art soft error aware CAD algorithms; Describes practical soft error aware synthesis techniques for commercial large-scale VLSI designs.