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Nota di contenuto	Configurable and In-Memory Accelerators -- Towards Multicore Performance with Configurable Computing Units -- Design and Evaluation of a Processing-in-Memory Architecture for the Smart Memory Cube -- Network-on-Chip and Secure Computing Architectures -- CASCADE: Congestion Aware Switchable Cycle Adaptive Detection Router -- An Alternating Transmission Scheme for Detection Routing based Network-on-Chips -- Exzess: Hardware-based RAM Encryption against Physical Memory Disclosure -- Hardware-Assisted Context Management for Accelerator Virtualization: A Case Study with RSA -- Cache Architectures and Protocols Adaptive

Cache Structures -- Optimization of a Linked Cache Coherence Protocol for Scalable Manycore Coherence -- Mapping of Applications on Heterogeneous -- Architectures and Real-Time Tasks on Multiprocessors Generic algorithmic scheme for 2D stencil applications on heterogeneous hybrid machines -- GPU-Accelerated BWA-MEM Genomic Mapping Algorithm Using Adaptive Load Balancing -- Task Variants with Different Scratchpad Memory Consumption in Multi-Task Environments -- Feedback-Based Admission Control for Hard Real-Time Task Allocation under Dynamic Workload on Many-core Systems -- All About Time: Timing, Tracing, and Performance Modeling Data Age Diminution in the Logical Execution Time Model -- Accurate Sample Time Reconstruction for Sensor Data Synchronization -- DiaSys: On-Chip Trace Analysis for Multi-Processor System-on-Chip -- Analysis of Intel's Haswell Microarchitecture Using The ECM Model and Microbenchmarks -- Measurement-Based Probabilistic Timing Analysis for Graphics Processor Units -- Approximate and Energy-Efficient Computing -- Reducing Energy Consumption of Data Transfers using Runtime Data Type Conversion -- Balancing High-Performance Parallelization and Accuracy in Canny Edge Detector -- Analysis and Exploitation of CTU-Level Parallelism in the HEVC Mode Decision Process Using Actor-based Modeling -- Low-Cost Hardware Infrastructure for Runtime Thread Level Energy Accounting -- Allocation: From Memories to FPGA Hardware Modules Reducing NoC and Memory Contention for Manycores -- An Efficient Data Structure for Dynamic Two-Dimensional Reconfiguration -- Organic Computing Systems Runtime Clustering of Similarly Behaving Agents in Open Organic Computing Systems -- Comparison of Dependency Measures for the Detection of Mutual Influences in Organic Computing Systems -- Augmenting the Algorithmic Structure of XCS by Means of Interpolation -- Reliability Aspects in NoCs, Caches, and GPUs Estimation of End-to-end Packet Error Rates for NoC Multicasts -- Protecting Code Regions on Asymmetrically Reliable Caches -- A New Simulation-based Fault Injection Approach for the Evaluation of Transient Errors in GPGPUs.

Sommario/riassunto

This book constitutes the proceedings of the 29th International Conference on Architecture of Computing Systems, ARCS 2016, held in Nuremberg, Germany, in April 2016. The 29 full papers presented in this volume were carefully reviewed and selected from 87 submissions. They were organized in topical sections named: configurable and in-memory accelerators; network-on-chip and secure computing architectures; cache architectures and protocols; mapping of applications on heterogeneous architectures and real-time tasks on multiprocessors; all about time: timing, tracing, and performance modeling; approximate and energy-efficient computing; allocation: from memories to FPGA hardware modules; organic computing systems; and reliability aspects in NoCs, caches, and GPUs.