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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Preliminaries -- An Open-Source RISC-V Evaluation Platform -- Formal Verification of SystemC-based Designs using Symbolic Simulation -- Coverage-guided Testing for Scalable Virtual Prototype Verification -- Verification of Embedded Software Binaries using Virtual Prototypes -- Validation of Firmware-Based Power Management using Virtual Prototypes -- Register-Transfer Level Correspondence Analysis -- Conclusion -- Index.
Sommario/riassunto	This book presents a comprehensive set of techniques that enhance all key aspects of a modern Virtual Prototype (VP)-based design flow. The authors emphasize automated formal verification methods, as well as advanced coverage-guided analysis and testing techniques, tailored for SystemC-based VPs and also the associated Software (SW). Coverage also includes VP modeling techniques that handle functional as well as non-functional aspects and also describes correspondence analyses between the Hardware- and VP-level to utilize information available at different levels of abstraction. All approaches are discussed in detail and are evaluated extensively, using several experiments to demonstrate their effectiveness in enhancing the VP-based design flow. Furthermore, the book puts a particular focus on the modern RISC-V ISA, with several case-studies covering modeling as well as VP and SW

verification aspects. Provides a comprehensive set of techniques to enhance all key aspects of a Virtual Prototype (VP)-based design flow Includes automated formal verification methods and advanced coverage-guided testing techniques, tailored for SystemC-based VPs Describes efficient, coverage-guided test generation methods for VP-based functional and non-functional software (SW) analysis and verification Includes correspondence analyses to utilize information between different abstraction levels in the design flow Uses several VP and SW verification case-studies that target the modern RISC-V ISA.