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Nota di contenuto	Keynote -- Platform Thinking in Embedded Systems -- Reconfigurable System Design and Implementations -- Interprocedural Optimization for Dynamic Hardware Configurations -- Reconfigurable Embedded Systems: An Application-Oriented Perspective on Architectures and Design Techniques -- Reconfigurable Multiple Operation Array -- RAPANUI: Rapid Prototyping for Media Processor Architecture Exploration -- Data-Driven Regular Reconfigurable Arrays: Design Space Exploration and Mapping -- Automatic FIR Filter Generation for FPGAs -- Two-Dimensional Fast Cosine Transform for Vector-STA Architectures -- Configurable Computing for High-Security/High-Performance Ambient Systems -- FPL-3E: Towards Language Support for Reconfigurable Packet Processing -- Processor Architectures, Design and Simulation -- Flux Caches: What Are They and Are They Useful? -- First-Level Instruction Cache Design for Reducing Dynamic Energy Consumption -- A Novel JAVA Processor for Embedded Devices -- Formal Specification of a Protocol Processor -- Tuning a Protocol Processor Architecture Towards DSP Operations -- Observations on Power-Efficiency Trends in Mobile Communication Devices -- CORDIC-Augmented Sandbridge Processor for Channel Equalization -- Power-Aware Branch Logic: A Hardware Based Technique for Filtering Access to Branch Logic -- Exploiting Intra-function Correlation with the Global

History Stack -- Power Efficient Instruction Caches for Embedded Systems -- Micro-architecture Performance Estimation by Formula -- Offline Phase Analysis and Optimization for Multi-configuration Processors -- Hardware Cost Estimation for Application-Specific Processor Design -- Ultra Fast Cycle-Accurate Compiled Emulation of Inorder Pipelined Architectures -- Generating Stream Based Code from Plain C -- Fast Real-Time Job Selection with Resource Constraints Under Earliest Deadline First -- A Programming Model for an Embedded Media Processing Architecture -- Automatic ADL-Based Assembler Generation for ASIP Programming Support -- Sandbridge Software Tools -- Architectures and Implementations -- A Hardware Accelerator for Controlling Access to Multiple-Unit Resources in Safety/Time-Critical Systems -- Pattern Matching Acceleration for Network Intrusion Detection Systems -- Real-Time Stereo Vision on a Reconfigurable System -- Application of Very Fast Simulated Reannealing (VFSR) to Low Power Design -- Compressed Swapping for NAND Flash Memory Based Embedded Systems -- A Radix-8 Multiplier Design and Its Extension for Efficient Implementation of Imaging Algorithms -- A Scalable Embedded JPEG2000 Architecture -- A Routing Paradigm with Novel Resources Estimation and Routability Models for X-Architecture Based Physical Design -- Benchmarking Mesh and Hierarchical Bus Networks in System-on-Chip Context -- DDM-CMP: Data-Driven Multithreading on a Chip Multiprocessor -- System Level Design, Modeling and Simulation -- Modeling NoC Architectures by Means of Deterministic and Stochastic Petri Nets -- High Abstraction Level Design and Implementation Framework for Wireless Sensor Networks -- The ODYSSEY Tool-Set for System-Level Synthesis of Object-Oriented Models -- Design and Implementation of a WLAN Terminal Using UML 2.0 Based Design Flow -- Rapid Implementation and Optimisation of DSP Systems on SoPC Heterogeneous Platforms -- DVB-DSNG Modem High Level Synthesis in an Optimized Latency Insensitive System Context -- SystemQ: A Queuing-Based Approach to Architecture Performance Evaluation with SystemC -- Moving Up to the Modeling Level for the Transformation of Data Structures in Embedded Multimedia Applications -- A Case for Visualization-Integrated System-Level Design Space Exploration -- Mixed Virtual/Real Prototypes for Incremental System Design – A Proof of Concept.

Sommario/riassunto

The SAMOS workshop is an international gathering of highly quali?ed researchers from academia and industry, sharing in a 3-day lively discussion on the quiet and - spiring northern mountainside of the Mediterranean island of Samos. As a tradition, the workshop features workshop presentations in the morning, while after lunch all kinds of informal discussions and nut-cracking gatherings take place. The workshop is unique in the sense that not only solved research problems are presented and discussed but also (partly) unsolved problems and in-depth topical reviews can be unleashed in the sci- ti?c arena. Consequently, the workshop provides the participants with an environment where collaboration rather than competition is fostered. The earlier workshops, SAMOS I–IV (2001–2004), were composed only of invited presentations. Due to increasing expressions of interest in the workshop, the Program Committee of SAMOS V decided to open the workshop for all submissions. As a result the SAMOS workshop gained an immediate popularity; a total of 114 submitted papers were received for evaluation. The papers came from 24 countries and regions: Austria (1), Belgium (2), Brazil (5), Canada (4), China (12), Cyprus (2), Czech Republic (1), Finland (15), France (6), Germany (8), Greece (5), Hong Kong (2), India (2), Iran (1), Korea (24), The Netherlands (7), Pakistan (1), Poland (2), Spain (2), Sweden (2), T- wan (1), Turkey (2), UK (2), and

USA (5). We are grateful to all of the authors who submitted papers to the workshop.