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Nota di contenuto	Compilers -- Runtime Biased Pointer Reuse Analysis and Its Application to Energy Efficiency -- Inter-program Compilation for Disk Energy Reduction -- Embedded Systems -- Energy Consumption in Mobile Devices: Why Future Systems Need Requirements–Aware Energy Scale-Down -- Efficient Scratchpad Allocation Algorithms for Energy Constrained Embedded Systems -- Online Prediction of Battery Lifetime for Embedded and Mobile Devices -- Synchroscalar: Initial Lessons in Power-Aware Design of a Tile-Based Embedded Architecture -- Heterogeneous Wireless Network Management -- Microarchitectural Techniques -- “Look It Up” or “Do the Math”: An Energy, Area, and Timing Analysis of Instruction Reuse and Memoization -- CPU Packing for Multiprocessor Power Reduction -- Exploring the Potential of Architecture-Level Power Optimizations -- Coupled Power and Thermal Simulation with Active Cooling -- Cache and Memory Systems -- The Synergy Between Power-Aware Memory Systems and Processor Voltage Scaling -- Hot-and-Cold: Using Criticality in the Design of Energy-Efficient Caches -- PARROT: Power Awareness Through Selective

Dynamically Optimized Traces.

Sommario/riassunto

Welcome to the proceedings of the 3rd Power-Aware Computer Systems (PACS 2003) Workshop held in conjunction with the 36th Annual International Symposium on Microarchitecture (MICRO-36). The increase in power and - ergy dissipation in computer systems has begun to limit performance and has also resulted in higher cost and lower reliability. The increase also implies - ducedbatterylifeinportablesystems. Becauseofthemagnitudeoftheproblem, alllevelsofcomputersystems, includingcircuits,architectures,andsoftware,are being employed to address power and energy issues. PACS 2003 was the third workshop in its series to explore power- and energy-awareness at all levels of computer systems and brought together experts from academia and industry. These proceedings include 14 research papers, selected from 43 submissions, spanningawidespectrumofareasinpower-awaresystems.Wehavegrouped the papers into the following categories: (1) compilers, (2) embedded systems, (3) microarchitectures, and (4) cache and memory systems. The ?rst paper on compiler techniques proposes pointer reuse analysis that is biased by runtime information (i.e., the targets of pointers are determined based on the likelihood of their occurrence at runtime) to map accesses to ener- e?cient memory access paths (e.g., avoid tag match). Another paper proposes compiling multiple programs together so that disk accesses across the programs can be synchronized to achieve longer sleep times in disks than if the programs are optimized separately.