

1.	Record Nr.	UNINA990005924960403321
	Autore	Calvitti, Pardo
	Titolo	Cenni di alcune delle circolari emanate dalla procura generale del Re presso la Corte d'Appello di Napoli dal 1885 al 1909 / Pardo Calvitti
	Pubbl/distr/stampa	Larino : Morrone, 1910
	Descrizione fisica	106 p. ; 24 cm
	Disciplina	345
	Locazione	FGBC
	Collocazione	MASSARI H 26
	Lingua di pubblicazione	Non definito
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
2.	Record Nr.	UNINA9910483059003321
	Titolo	Automated technology for verification and analysis : third international symposium, ATVA 2005, Taipei, Taiwan, October 4-7, 2005 : proceedings / / Doron A. Peled, Yih-Kuen Tsay (eds.)
	Pubbl/distr/stampa	Berlin, : Springer, 2005
	Edizione	[1st ed. 2005.]
	Descrizione fisica	1 online resource (XII, 508 p.)
	Collana	Lecture notes in computer science, , 0302-9743 ; ; 3707
	Altri autori (Persone)	PeledDoron <1962-> TsayYih-Kuen <1962->
	Disciplina	620.00420285
	Soggetti	Automatic theorem proving
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Bibliographic Level Mode of Issuance: Monograph
	Nota di bibliografia	Includes bibliographical references and index.
	Nota di contenuto	Keynote Speeches -- Ranking Abstraction as a Companion to Predicate Abstraction -- Termination and Invariance Analysis of Loops -- Some Perspectives of Infinite-State Verification -- Model Checking --

Verifying Very Large Industrial Circuits Using 100 Processes and Beyond
 -- A New Reachability Algorithm for Symmetric Multi-processor Architecture -- Comprehensive Verification Framework for Dependability of Self-optimizing Systems -- Exploiting Hub States in Automatic Verification -- Combined Methods -- An Approach for the Verification of SystemC Designs Using AsmL -- Decomposition-Based Verification of Cyclic Workflows -- Timed, Embedded, and Hybrid Systems (I) -- Guaranteed Termination in the Verification of LTL Properties of Non-linear Robust Discrete Time Hybrid Systems -- Computation Platform for Automatic Analysis of Embedded Software Systems Using Model Based Approach -- Quantitative and Qualitative Analysis of Temporal Aspects of Complex Activities -- Automatic Test Case Generation with Region-Related Coverage Annotations for Real-Time Systems -- Abstraction and Reduction Techniques -- Selective Search in Bounded Model Checking of Reachability Properties -- Predicate Abstraction of RTL Verilog Descriptions Using Constraint Logic Programming -- State Space Exploration of Object-Based Systems Using Equivalence Reduction and the Sweepline Method -- Syntactical Colored Petri Nets Reductions -- Decidability and Complexity -- Algorithmic Algebraic Model Checking II: Decidability of Semi-algebraic Model Checking and Its Applications to Systems Biology -- A Static Analysis Using Tree Automata for XML Access Control -- Reasoning About Transfinite Sequences -- Semi-automatic Distributed Synthesis -- Established Formalisms and Standards -- A New Graph of Classes for the Preservation of Quantitative Temporal Constraints -- Comparison of Different Semantics for Time Petri Nets -- Introducing Dynamic Properties with Past Temporal Operators in the B Refinement -- Approximate Reachability for Dead Code Elimination in Esterel??? -- Compositional Verification and Games -- Synthesis of Interface Automata -- Multi-valued Model Checking Games -- Timed, Embedded, and Hybrid Systems (II) -- Model Checking Prioritized Timed Automata -- An MTBDD-Based Implementation of Forward Reachability for Probabilistic Timed Automata -- Protocols Analysis, Case Studies, and Tools -- An EFSM-Based Intrusion Detection System for Ad Hoc Networks -- Modeling and Verification of a Telecommunication Application Using Live Sequence Charts and the Play-Engine Tool -- Formal Construction and Verification of Home Service Robots: A Case Study -- Model Checking Real Time Java Using Java PathFinder -- Infinite-State and Parameterized Systems -- Using Parametric Automata for the Verification of the Stop-and-Wait Class of Protocols -- Flat Acceleration in Symbolic Model Checking -- Flat Counter Automata Almost Everywhere!.

Sommario/riassunto

The Automated Technology for Verification and Analysis (ATVA) international symposium series was initiated in 2003, responding to a growing interest in formal verification spurred by the booming IT industry, particularly hardware design and manufacturing in East Asia. Its purpose is to promote research on automated verification and analysis in the region by providing a forum for interaction between the regional and the international research/industrial communities of the field. ATVA 2005, the third of the ATVA series, was held in Taipei, Taiwan, October 4–7, 2005. The main theme of the symposium encompasses design, complexities, tools, and applications of automated methods for verification and analysis. The symposium was co-located and had a two-day overlap with FORTE 2005, which was held October 2–5, 2005. We received a total of 95 submissions from 17 countries. Each submission was assigned to three Program Committee members, who were helped by their subreviewers, for rigorous and fair evaluation. The final deliberation by the Program Committee was

conducted over email for a duration of about 10 days after nearly all review reports had been collected. In the end, 33 papers were - lectedforinclusioninthe program.

ATVA2005hadthreekeynotespeechesgiven respectively by Amir Pnueli (joint with FORTE 2005), Zohar Manna, and Wolfgang Thomas. The main symposium was preceded by a tutorial day, consisting of three two-hour lectures given also by the keynote speakers.
