Record Nr. UNINA9910480182803321 Autore Wang Laung-Terng Titolo Electronic design automation [[electronic resource]]: synthesis, verification, and test // edited by Laung-Terng Wang, Yao-Wen Chang, Kwang-Ting (Tim) Cheng Amsterdam,: Morgan Kaufmann/Elsevier, c2009 Pubbl/distr/stampa **ISBN** 1-282-54215-X 9786612542152 0-08-092200-7 Edizione [1st edition] Descrizione fisica 1 online resource (971 p.) The Morgan Kaufmann series in systems on silicon Collana Altri autori (Persone) WangLaung-Terng ChangYao-Wen <1966-> ChengKwang-Ting <1961-> 621.3810285 Disciplina 621.39/5 22 Soggetti Electronic circuit design - Data processing Computer-aided design Electronic books. Lingua di pubblicazione Inglese **Formato** Materiale a stampa Livello bibliografico Monografia Note generali Description based upon print version of record. Nota di bibliografia Includes bibliographical references and index. Nota di contenuto Front Cover; Electronic Design Automation: Synthesis, Verification, and Test: Copyright Page: Contents: Preface: In the Classroom: Acknowledgments; Contributors; About the Editors; CHAPTER 1 Introduction; 1.1 Overview of electronic design automation; 1.2 Logic design automation; 1.3 Test automation; 1.4 Physical design automation; 1.5 Concluding remarks; 1.6 Exercises; Acknowledgments; References; CHAPTER 2 Fundamentals of CMOS design; 2.1 Introduction; 2.2 Integrated circuit technology; 2.3 CMOS logic; 2.4 Integrated circuit design techniques; 2.5 CMOS physical design 2.6 Low-power circuit design techniques 2.7 Concluding remarks; 2.8 Exercises; Acknowledgments; References; CHAPTER 3 Design for testability; 3.1 Introduction; 3.2 Testability analysis; 3.3 Scan design; 3.4 Logic built-in self-test; 3.5 Test Compression; 3.6 Concluding remarks; 3.7 Exercises; Acknowledgments; References; CHAPTER 4

Fundamentals of algorithms; 4.1 Introduction; 4.2 Computational

complexity; 4.3 Graph algorithms; 4.4 Heuristic algorithms; 4.5 Mathematical programming; 4.6 Concluding remarks; 4.7 Exercises; Acknowledgments; References

CHAPTER 5 Electronic system-level design and high-level synthesis5.1 Introduction; 5.2 Fundamentals of High-level synthesis; 5.3 High-level synthesis algorithm overview; 5.4 Scheduling; 5.5 Register binding; 5.6 Functional unit binding: 5.7 Concluding remarks: 5.8 Exercises: Acknowledgments; References; CHAPTER 6 Logic synthesis in a nutshell; 6.1 Introduction; 6.2 Data Structures for Boolean representation and reasoning; 6.3 Combinational logic minimization; 6.4 Technology mapping; 6.5 Timing analysis; 6.6 Timing optimization; 6.7 Concluding remarks; 6.8 Exercises; Acknowledgments ReferencesCHAPTER 7 Test synthesis; 7.1 Introduction; 7.2 Scan design; 7.3 Logic built-in self-test (BIST) design.; 7.4 RTL Design for testability: 7.5 Concluding remarks: 7.6 Exercises: Acknowledgments: References; CHAPTER 8 Logic and circuit simulation; 8.1 Introduction; 8.2 Logic simulation models; 8.3 Logic simulation techniques; 8.4 Hardware-accelerated logic simulation; 8.5 Circuit simulation models; 8.6 Numerical methods for transient analysis; 8.7 Simulation of VLSI interconnects; 8.8 Simulation of nonlinear devices; 8.9 Concluding remarks: 8.10 Exercises: Acknowledgments: References CHAPTER 9 Functional verification 9.1 Introduction; 9.2 Verification hierarchy; 9.3 Measuring verification quality; 9.4 Simulation-based approach; 9.5 Formal approaches; 9.6 Advanced research; 9.7 Concluding remarks; 9.8 Exercises; Acknowledgments; References; CHAPTER 10 Floorplanning; 10.1 Introduction; 10.2 Simulated annealing approach; 10.3 Analytical approach; 10.4 Modern floorplanning considerations; 10.5 Concluding remarks; 10.6 Exercises; Acknowledgments; References; CHAPTER 11 Placement; 11.1 Introduction: 11.2 Problem formulations: 11.3 Global placement: partitioning-based approach 11.4 Global placement: simulated annealing approach

Sommario/riassunto

This book provides broad and comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an ""adjacent"" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book. Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verific