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Nota di contenuto	CONTENTS; Preface; Low-Noise Measurements of Small Currents and Voltages for Characterization of Semiconductor Nanostructures at Low Temperatures J. Jacob and B. Fiedler; 1. Introduction; 2. Multi-Channel Pre-Amplification and Signal Conditioning System; 2.1. Input Amplifier Module; 2.2. Preliminary Filtering; 2.3. Universal Filter Matrix; 2.4. Output Stage; 2.5. Control and Power Supply; 2.6. Circuit Board Design; 2.7. Performance; 3. Battery-Powered Current and Voltage Amplification for Ultra-Low-Noise Measurements; 4. Conclusion; Acknowledgment; References An Integrated Approach to Power Quality Problems in Micro-Grids Tsao-Tsung Ma1. Introduction; 2. Micro-grid and Control Techniques; 2.1. Micro-grid Concepts and Power Quality Issues; 2.2. Control Techniques; 2.3. Calculation of Reference Current Commands; 3. Case Studies and Results; 3.1. Simulation Cases and Results; 3.2. Experimental Tests and Results; 4. Conclusion; Acknowledgments; References; Discriminating Among Inrush Current, External Short Circuit and Internal Winding Fault in Power Transformer Using Coefficient of DWT Jittiphong Klomjit and Atthapol Ngaopitakkul; 1. Introduction

2. Wavelet Transform; 3. Power System Simulation using EMTP; 4. Fault Detection Algorithm; 5. Conclusion; Acknowledgments; References; Classification of Temporal Characteristics of Epileptic EEG Subbands Based on the Local Maxima S. Janjarasjitt; 1. Introduction; 2. Methods; 2.1. Data and Subjects; 2.2. The Local Maxima and the Temporal Characteristics; 2.3. Analytical Framework; 3. Results; 4. Conclusions and Discussion; Acknowledgments; References

A Concurrent Error Detection and Correction Based Fault-Tolerant XOR-XNOR Circuit for Highly Reliable Applications Mouna Karmani, Chiraz Khedhiri, Belgacem Hamdi, Ka Lok Man, Eng Gee Lim and Chi-Un Lei; 1. Introduction; 2. Concurrent Error Detection and Correction Based Fault-Tolerant Systems; 2.1. The proposed XOR-XNOR circuit implementation; 2.2. Simulation results; 3. The XOR-XNOR Circuit Fault Analysis; 3.1. The stuck-at fault model; 3.2. The transistor stuck-on fault model; 3.3. The transistor stuck-on fault model; 4. The Proposed Concurrent Error Correction Architecture; 5. Conclusion

References

Probability Distributions on an AND-OR Tree Under Directional Algorithms Toshio Suzuki and Ryota Nakamura; 1. Introduction; 2. Notation; 3. The equivalence of eigen and E1; 4. A case where the uniqueness fails; 5. A case where the uniqueness holds; 6. Conclusive remarks; Acknowledgment; References; An Efficient Differential Full Adder Chiraz Khedhiri, Mouna Karmani, Belgacem Hamdi and Ka Lok Man; 1. Introduction; 1.1. The CMOS full adder; 1.2. The TGA full adder; 1.3. The Complementary Pass Transistor Logic (CPL) full adder; 1.4. The Double Pass transistor Logic (DPL) full adder; 1.5. The full adder in combined technology (CMOS+ DPL)

Sommario/riassunto

This volume contains revised and extended research articles written by prominent researchers. Topics covered include electrical engineering, circuits, artificial intelligence, data mining, imaging engineering, bioinformatics, internet computing, software engineering, and industrial applications. The book offers tremendous state-of-the-art advances in electrical engineering and also serves as an excellent reference work for researchers and graduate students working with/on electrical engineering.
