Record Nr. UNINA9910465210403321 VLSI and computer architecture [[electronic resource] /] / Kenzo **Titolo** Watanabe, editor New York, : Nova Science Publisher, c2009 Pubbl/distr/stampa **ISBN** 1-61209-883-5 Descrizione fisica 1 online resource (253 p.) Altri autori (Persone) WatanabeKenzo Disciplina 621.39/5 Soggetti Integrated circuits - Very large scale integration - Design and construction Computer architecture Wireless communication systems - Equipment and supplies - Design and construction Microcontrollers - Design and construction Electronic books. Lingua di pubblicazione Inglese **Formato** Materiale a stampa Livello bibliografico Monografia Note generali Description based upon print version of record. Nota di bibliografia Includes bibliographical references and index. ""VLSI AND COMPUTERARCHITECTURE""; ""VLSI AND COMPUTER Nota di contenuto ARCHITECTURE ""; ""CONTENTS""; ""PREFACE""; ""DESIGN CONSIDERATIONS AND ALGORITHMSFOR BROADBAND FIXED WIMAX SYSTEMS""; ""Abstract""; ""1. Introduction""; ""1.1. Introduction""; ""1.2. Orthogonal Frequency Division Multiplexing (OFDM)""; ""1.2.1. Noniterative OFDM Scheme""; ""1.2.2. Iterative OFDM Scheme""; ""1.3. SC-FDE""; ""1.4. Quantitative Results""; ""2. Time-Domain Solutions""; ""2.1. Time-Domain Turbo Equalization for SISO System""; ""2.1.1. Initial stage""; ""2.1.2. Subsequent Stages""; ""2.1.3. Complexity Comparison"" ""2.2. Time-Domain Turbo Equalization for MIMO Systems"""2.2.1. Initial Stage""; ""2.2.2. Subsequent Stages""; ""2.3. Performance Comparison""; ""3. Conclusions""; ""References""; ""VLSI INTERCONNECTS AND THEIR DELAYPERFORMANCE": ""Abstract"": ""1. Introduction""; ""2. Modeling Interconnect as RC & RLC Circuits""; ""2.1. Lumped and Distributed Models""; ""3. Extraction of Interconnect Parasitics""; ""4. Propagation Delay through Driver Interconnect Load Model""; ""4.1. Driver Delay Models""; ""4.2. Interconnect Delay

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