

1. Record Nr.	UNINA9910463996303321
Autore	Maziad Samar
Titolo	Monetary policy and the Central Bank in Jordan [[electronic resource] /] / Samar Maziad
Pubbl/distr/stampa	[Washington, D.C.], : International Monetary Fund, Strategy, Policy, and Review Dept., 2009
ISBN	1-4623-1944-0 9786612844003 1-4527-8941-X 1-282-84400-8 1-4518-7338-7
Descrizione fisica	29 p. : ill
Collana	IMF working paper ; ; WP/09/191
Soggetti	Monetary policy - Jordan - Econometric models Financial crises - Jordan - Econometric models Banks and banking, Central - Jordan - Econometric models Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"August 2009."

2. Record Nr.	UNISA996465663003316
Titolo	Correct hardware design and verification methods : 10th IFIP WG10.5 advanced research working conference, CHARME'99, Bad Herrenalb, Germany, September 27-29, 1999 : proceedings / / Laurence Pierre, Thomas Kropf (editors)
Pubbl/distr/stampa	Berlin : , : Springer, , [1999] Â©1999
ISBN	3-540-48153-2
Edizione	[1st ed. 1999.]
Descrizione fisica	1 online resource (XII, 376 p.)
Collana	Lecture notes in computer science ; ; 1703
Disciplina	621.395
Soggetti	Integrated circuits - Very large scale integration - Computer-aided design Integrated circuits - Verification
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Invited Talks -- Esterel and Jazz : Two Synchronous Languages for Circuit Design -- Design Process of Embedded Automotive Systems—Using Model Checking for Correct Specifications -- Proof of Microprocessors -- A Proof of Correctness of a Processor Implementing Tomasulo's Algorithm without a Reorder Buffer -- Formal Verification of Explicitly Parallel Microprocessors -- Superscalar Processor Verification Using Efficient Reductions of the Logic of Equality with Uninterpreted Functions to Propositional Logic -- Model Checking -- Model Checking TLA+ Specifications -- Efficient Decompositional Model Checking for Regular Timing Diagrams -- Vacuity Detection in Temporal Model Checking -- Formal Methods and Industrial Applications -- Using Symbolic Model Checking to Verify the Railway Stations of Hoorn-Kersenboogerd and Heerhugowaard -- Practical Application of Formal Verification Techniques on a Frame Mux/Demux Chip from Nortel Semiconductors -- Efficient Verification of Timed Automata Using Dense and Discrete Time Semantics -- Abstraction and Compositional Techniques -- From Asymmetry to Full Symmetry: New Techniques for Symmetry Reduction in Model Checking -- Automatic Error Correction of Large Circuits Using Boolean Decomposition and

Abstraction -- Abstract BDDs: A Technique for Using Abstraction in
 Model Checking -- Theorem Proving Related Approaches -- Formal
 Synthesis at the Algorithmic Level -- Xs Are for Trajectory Evaluation,
 Booleans Are for Theorem Proving -- Verification of Infinite State
 Systems by Compositional Model Checking -- Symbolic
 Simulation/Symbolic Traversal -- Formal Verification of Designs with
 Complex Control by Symbolic Simulation -- Hints to Accelerate
 Symbolic Traversal -- Specification Languages and Methodologies --
 Modeling and Checking Networks of Communicating Real-Time
 Processes -- "Have I Written Enough Properties?" - A Method of
 Comparison Between Specification and Implementation -- Program
 Slicing of Hardware Description Languages -- Posters -- Results of the
 Verification of a Complex Pipelined Machine Model -- Hazard—
 Freedom Checking in Speed—Independent Systems -- Yet Another
 Look at LTL Model Checking -- Verification of Finite-State-Machine
 Refinements Using a Symbolic Methodology -- Refinement and
 Property Checking in High-Level Synthesis Using Attribute Grammars
 -- A Systematic Incrementalization Technique and Its Application to
 Hardware Design -- Bisimulation and Model Checking -- Circular
 Compositional Reasoning about Liveness -- Symbolic Simulation of
 Microprocessor Models Using Type Classes in Haskell -- Exploiting
 Retiming in a Guided Simulation Based Validation Methodology -- Fault
 Models for Embedded Systems -- Validation of Object-Oriented
 Concurrent Designs by Model Checking.

Sommario/riassunto

CHARME'99 is the tenth in a series of working conferences devoted to
 the development and use of leading-edge formal techniques and tools
 for the design and verification of hardware and systems. Previous
 conferences have been held in Darmstadt (1984), Edinburgh (1985),
 Grenoble (1986), Glasgow (1988), Leuven (1989), Torino (1991), Arles
 (1993), Frankfurt (1995) and Montreal (1997). This workshop and
 conference series has been organized in cooperation with IFIP WG 10.
 5. It is now the biannual counterpart of FMCAD, which takes place every
 even-numbered year in the USA. The 1999 event took place in Bad Her-
 nalb, a resort village located in the Black Forest close to the city of
 Karlsruhe. The validation of functional and timing behavior is a major
 bottleneck in current VLSI design systems. A predominantly academic
 area of study until a few years ago, formal design and verification
 techniques are now migrating into industrial use. The aim of CHARME'
 99 is to bring together researchers and users from academia and
 industry working in this active area of research. Two invited talks
 illustrate major current trends: the presentation by Gérard Berry (Ecole
 des Mines de Paris, Sophia-Antipolis, France) is concerned with the use
 of synchronous languages in circuit design, and the talk given by Peter
 Jansen (BMW, Munich, Germany) demonstrates an application of formal
 methods in an industrial environment. The program also includes 20
 regular presentations and 12 short presentations/poster exhibitions
 that have been selected from the 48 submitted papers.

3. Record Nr.	UNISANNIOMIL0184566	
Titolo	Il Medioevo / a cura di Giovanni Pugliese Carratelli	
Pubbl/distr/stampa	[Napoli], : Electa Napoli, ©1992 (, stampa 1993)	
Descrizione fisica	455 p. : ill. ; 29 cm	
Disciplina	700.947 945.72 945.7202	
Soggetti	CAMPANIA - Storia - Sec. 5.-14 ARTE - Campania - Storia - Sec. 5.-14 CAMPANIA - STORIA - MEDIOEVO - SAGGI CAMPANIA - VITA ARTISTICA E CULTURALE - MEDIOEVO - SAGGI	
Collocazione	POZZO LIB.ECON MON 981201STORICA 9	981201POZZO LIB.ECON MON STOECD
Lingua di pubblicazione	Italiano	
Formato	Materiale a stampa	
Livello bibliografico	Monografia	
Note generali	In custodia.	