1. Record Nr. UNINA9910462306603321

Autore	Smit Anneke
Titolo	The property rights of refugees and internally displaced persons : beyond restitution / / Anneke Smit
Pubbl/distr/stampa	Abingdon [England] ; ; New York : , : Routledge, , 2012
ISBN	1-280-68161-6 9786613658555 1-136-33144-1 0-203-12219-4
Descrizione fisica	1 online resource (267 p.)
Disciplina	341.4/86
Soggetti	Refugees - Legal status, laws, etc Internally displaced person - Legal status, laws, etc Restitution Repatriation Right of property Refugees - Housing Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"A GlassHouse book."
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	The development of the right to return to one's home of origin -- Modern experiences with post-conflict restitution and return -- Restitution and return "home" -- Local integration and the regularization of collective centre space -- Compensation and regularizing secondary occupation.
Sommario/riassunto	The Property Rights of Refugees and Internally Displaced Persons: Beyond Restitution explores how the protection of housing and property rights can contribute to durable solutions to displacement. The focus of most of the international community's recent protection efforts has been on returning displaced persons to their homes following armed conflict. ?This prioritization has been entrenched further by the 2005 United Nations Principles on Housing and Property Restitution for Refugees and Displaced Persons (the ""Pinheiro

Principles""). Yet as Anneke Smit chronicles in this book, the internat

2. Record Nr. UNINA9910484390303321

Titolo	Advances in Computer Systems Architecture : 12th Asia-Pacific Conference, ACSAC 2007, Seoul, Korea, August 23-25, 2007, Proceedings / / edited by Lynn Choi, Yunheung Paek, Sangyeun Cho
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2007
ISBN	1-281-04270-6 9786611042707 3-540-74309-X
Edizione	[1st ed. 2007.]
Descrizione fisica	1 online resource (XIII, 402 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 4697
Disciplina	004
Soggetti	Computer systems Computer arithmetic and logic units Computer input-output equipment Logic design Computer networks Microprocessors Computer architecture Computer System Implementation Arithmetic and Logic Structures Input/Output and Data Communications Logic Design Computer Communication Networks Processor Architectures
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	A Compiler Framework for Supporting Speculative Multicore Processors -- Power-Efficient Heterogeneous Multicore Technology for Digital Convergence -- StarDBT: An Efficient Multi-platform Dynamic Binary

Translation System -- Unbiased Branches: An Open Problem -- An Online Profile Guided Optimization Approach for Speculative Parallel Threading -- Entropy-Based Profile Characterization and Classification for Automatic Profile Management -- Laplace Transformation on the FT64 Stream Processor -- Towards Data Tiling for Whole Programs in Scratchpad Memory Allocation -- Evolution of NAND Flash Memory Interface -- FCC-SDP: A Fast Close-Coupled Shared Data Pool for Multi-core DSPs -- Exploiting Single-Usage for Effective Memory Management -- An Alternative Organization of Defect Map for Defect-Resilient Embedded On-Chip Memories -- An Effective Design of Master-Slave Operating System Architecture for Multiprocessor Embedded Systems -- Optimal Placement of Frequently Accessed IPs in Mesh NoCs -- An Efficient Link Controller for Test Access to IP Core-Based Embedded System Chips -- Performance of Keyword Connection Algorithm in Nested Mobility Networks -- Leakage Energy Reduction in Cache Memory by Software Self-invalidation -- Exploiting Task Temperature Profiling in Temperature-Aware Task Scheduling for Computational Clusters -- Runtime Performance Projection Model for Dynamic Power Management -- A Power-Aware Alternative for the Perceptron Branch Predictor -- Power Consumption and Performance Analysis of 3D NoCs -- A Design Methodology for Performance-Resource Optimization of a Generalized 2D Convolution Architecture with Quadrant Symmetric Kernels -- Bipartition Architecture for Low Power JPEG Huffman Decoder -- A SWP Specification for Sequential Image Processing Algorithms -- A Stream System-on-ChipArchitecture for High Speed Target Recognition Based on Biologic Vision -- FPGA-Accelerated Active Shape Model for Real-Time People Tracking -- Performance Evaluation of Evolutionary Multi-core and Aggressively Multi-threaded Processor Architectures -- Synchronization Mechanisms on Modern Multi-core Architectures -- Concerning with On-Chip Network Features to Improve Cache Coherence Protocols for CMPs -- Generalized Wormhole Switching: A New Fault-Tolerant Mathematical Model for Adaptively Wormhole-Routed Interconnect Networks -- Open Issues in MPI Implementation -- Implicit Transactional Memory in Kilo-Instruction Multiprocessors -- Design of a Low–Power Embedded Processor Architecture Using Asynchronous Function Units -- A Bypass Mechanism to Enhance Branch Predictor for SMT Processors -- Thread Priority-Aware Random Replacement in TLBs for a High-Performance Real-Time SMT Processor -- Architectural Solution to Object-Oriented Programming.

Sommario/riassunto

On behalf of the program and organizing committee members of this conference, we th are pleased to present you with the proceedings of the 12 Asia-Pacific Computer Systems Architecture Conference (ACSAC 2007), which was hosted in Seoul, Korea on August 23-25, 2007. This conference has traditionally been a forum for leading researchers in the Asian, American and Oceanian regions to share recent progress and the latest results in both architectural and system issues. In the past few years the c- ference has become more international in the sense that the geographic origin of p- ticipants has become broader to include researchers from all around the world, incl- ing Europe and the Middle East. This year, we received 92 paper submissions. Each submission was reviewed by at least three primary reviewers along with up to three secondary reviewers. The total number of completed reviews reached 333, giving each submission 3.6 reviews on average. All the reviews were carefully examined during the paper selection process, and finally 26 papers were accepted, resulting in an acceptance rate of about 28%. The selected papers encompass a wide range of topics, with much emphasis on hardware and software techniques for state-of-the-art

multicore and multithreaded architectures.